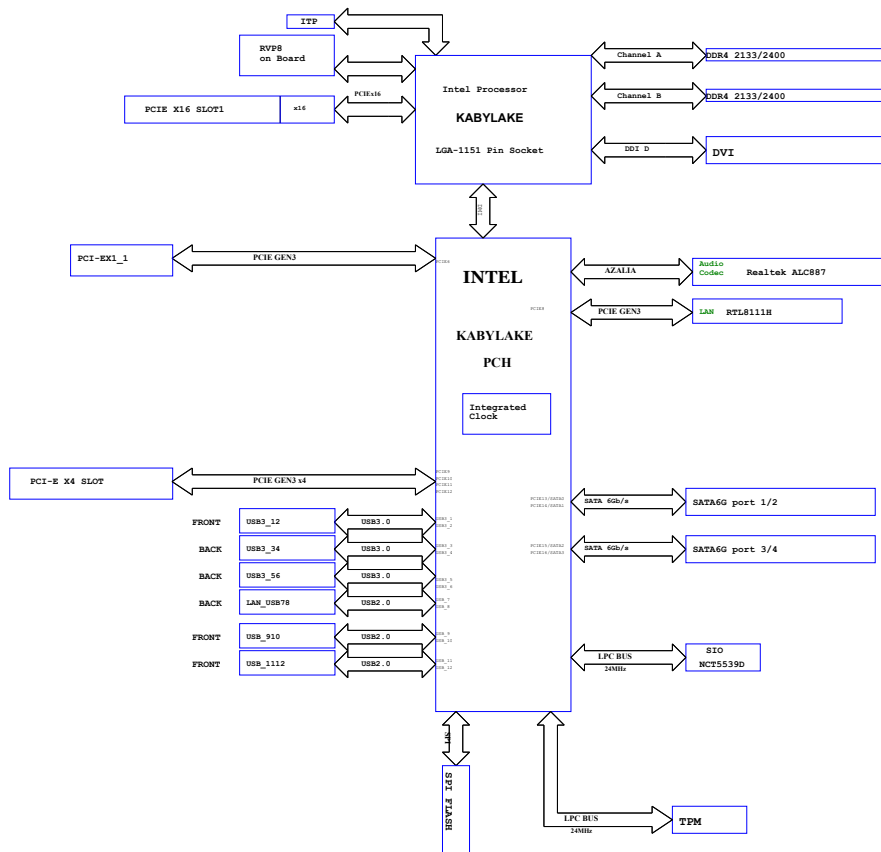
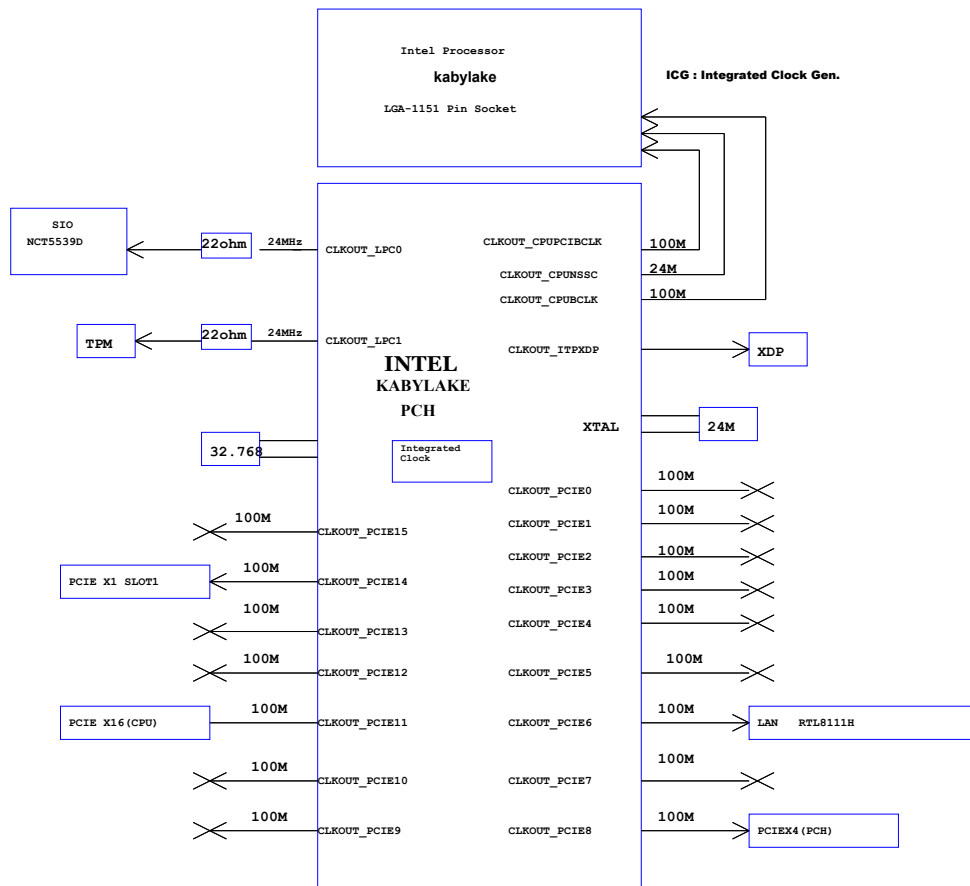
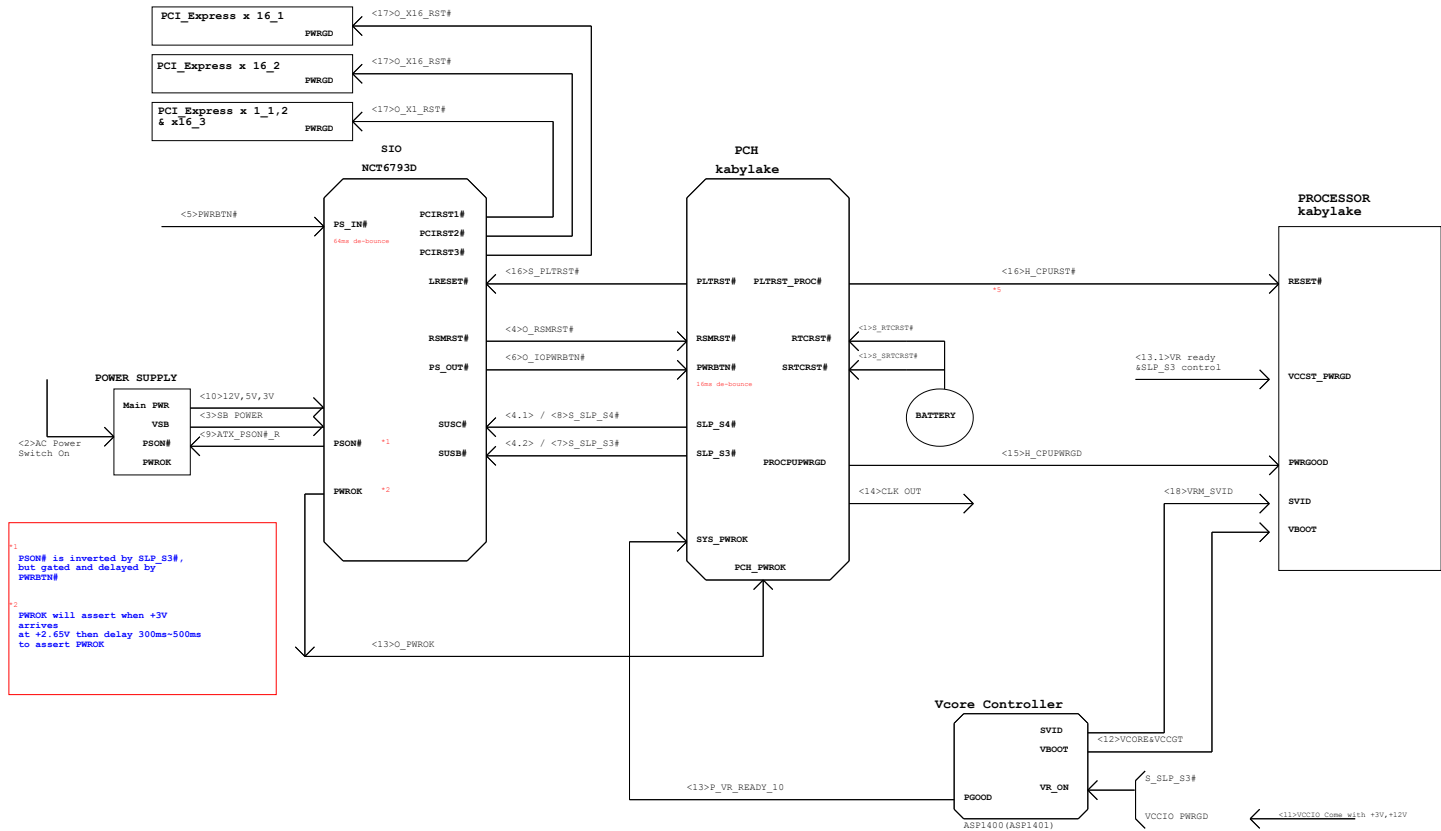


# EX-B250M-V3

Rev 1.02

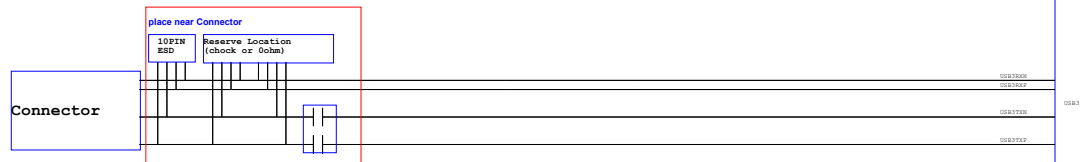
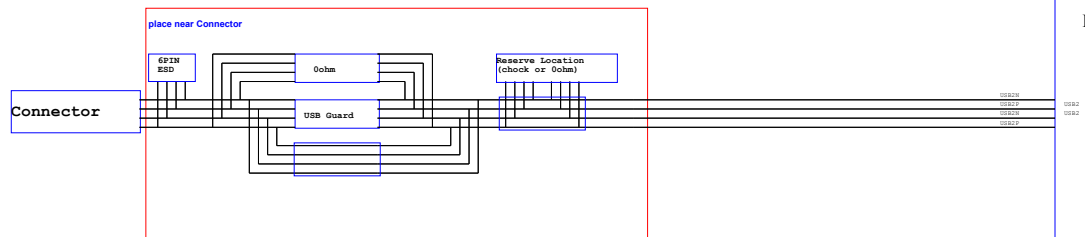


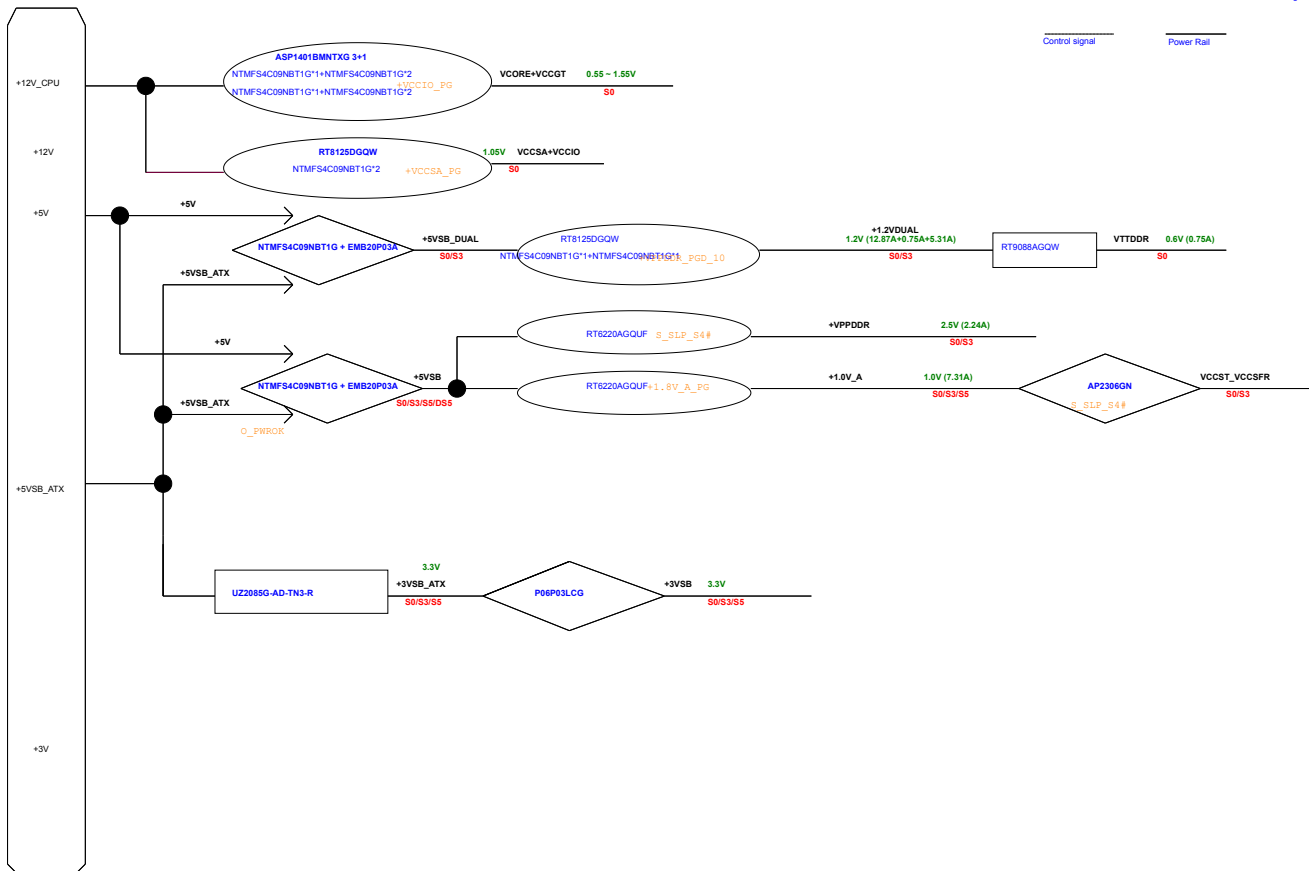
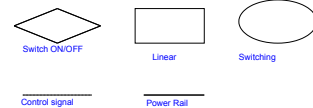




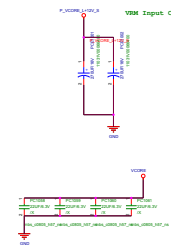
INTEL

KABYLAKE  
PCH



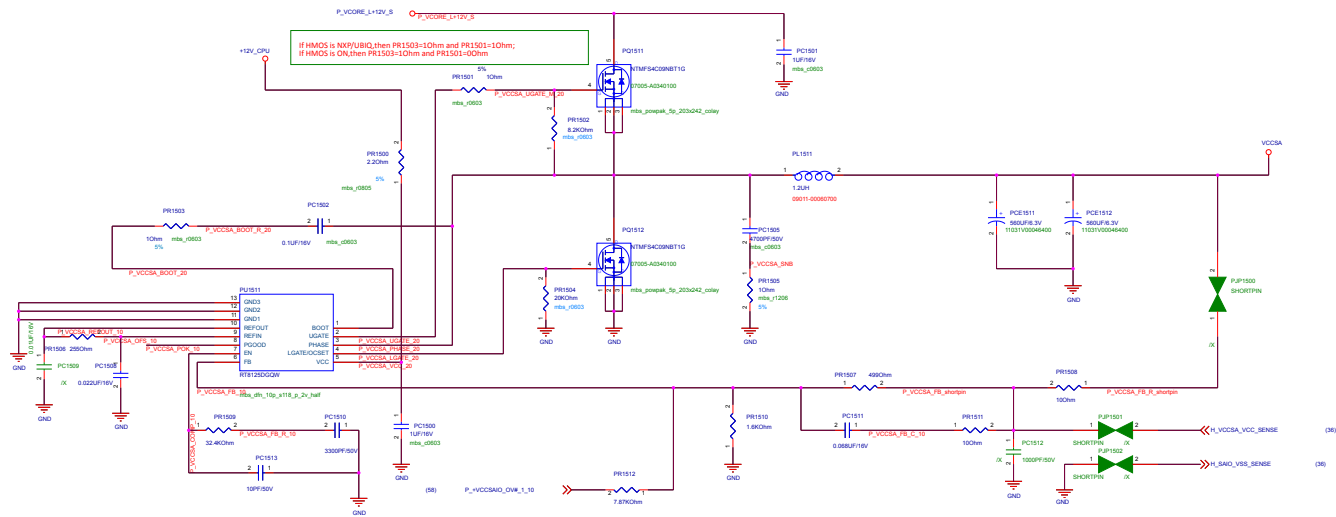




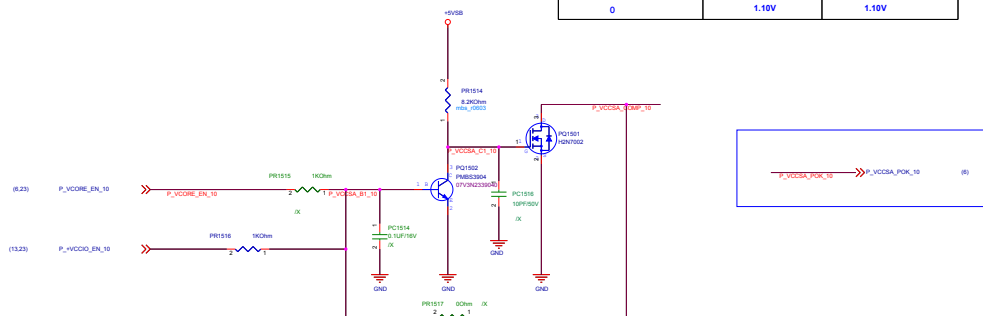


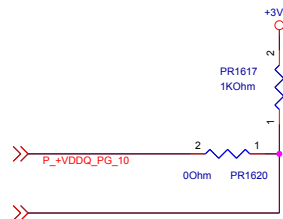


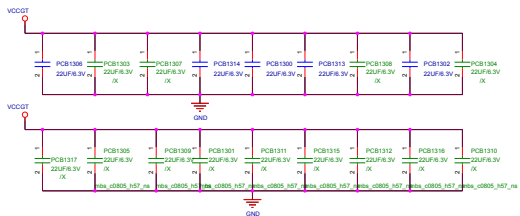
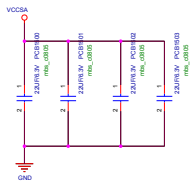


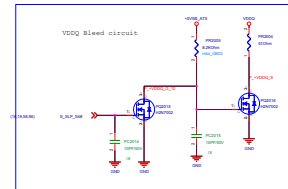
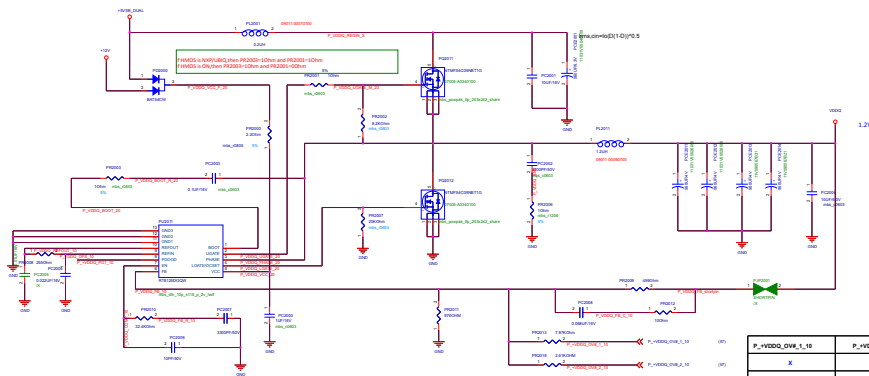


P_VCCSA_OVR_1_10	VCCSA show value	VCCSA show value
1	1.00V(default)	1.00V
0	1.10V	1.10V

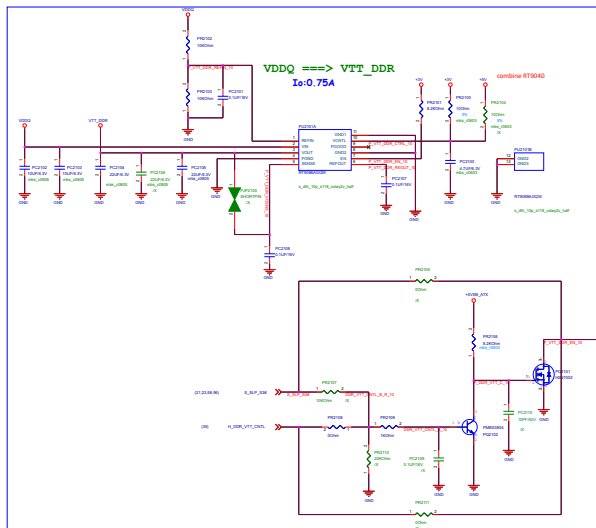


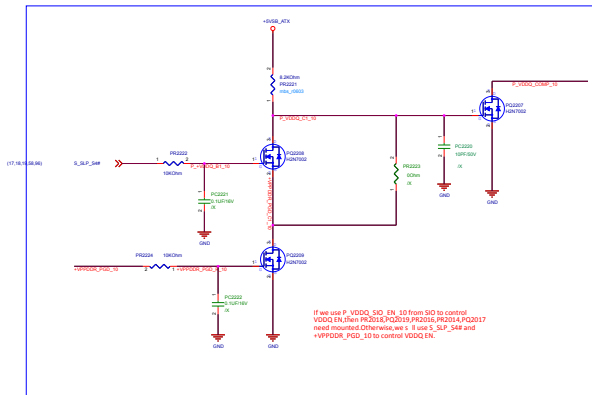
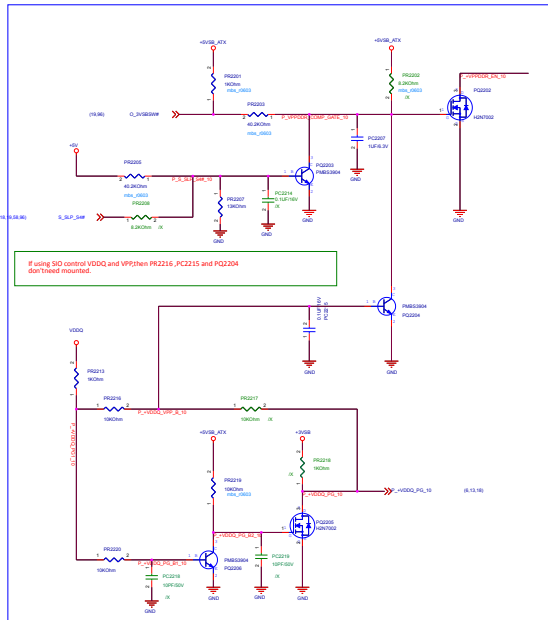
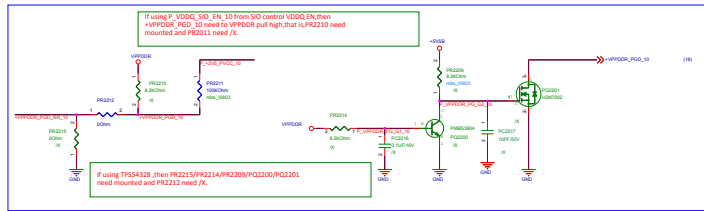
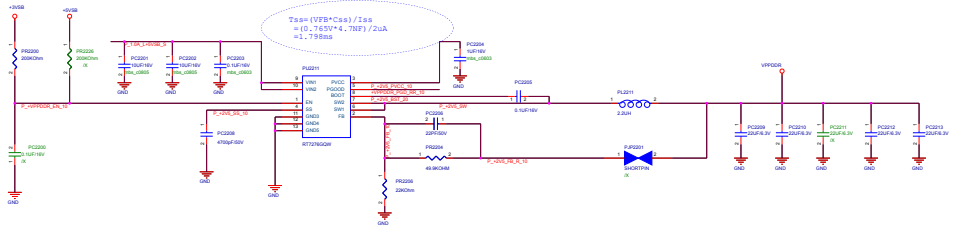




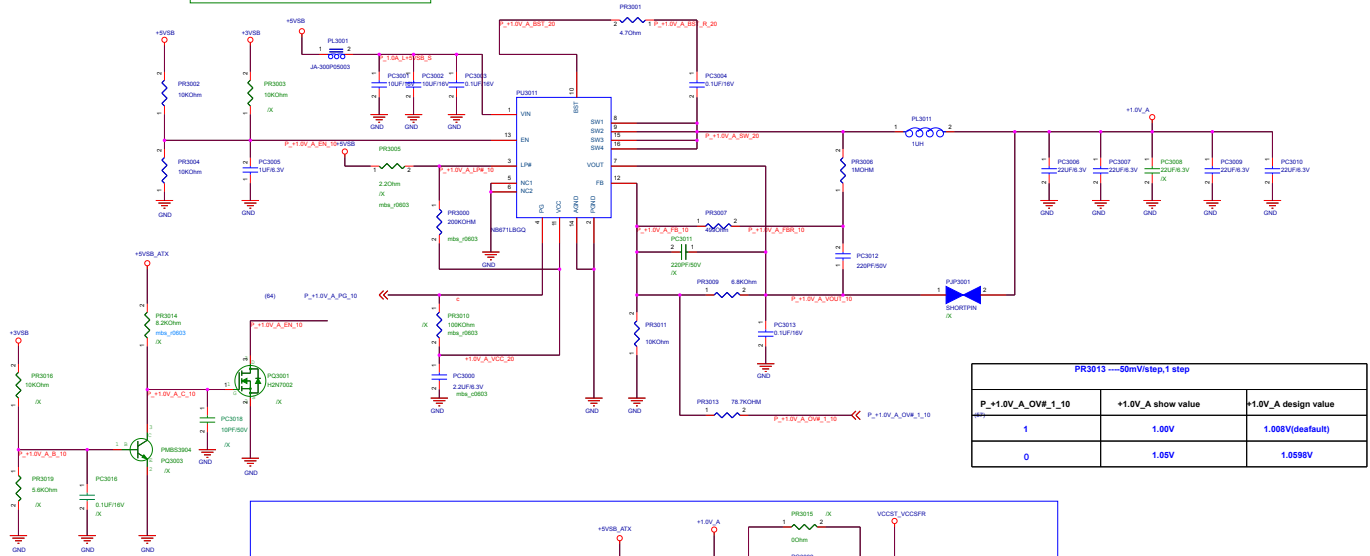


P_VDDQ_OV1_10	P_VDDQ_OV1_10	VDDQ show value	VDDQ design value
X	X	1.2V	1.280V
0	X	1.28V	1.280V
X	0	1.28V	1.320V
0	0	1.4V	1.410V



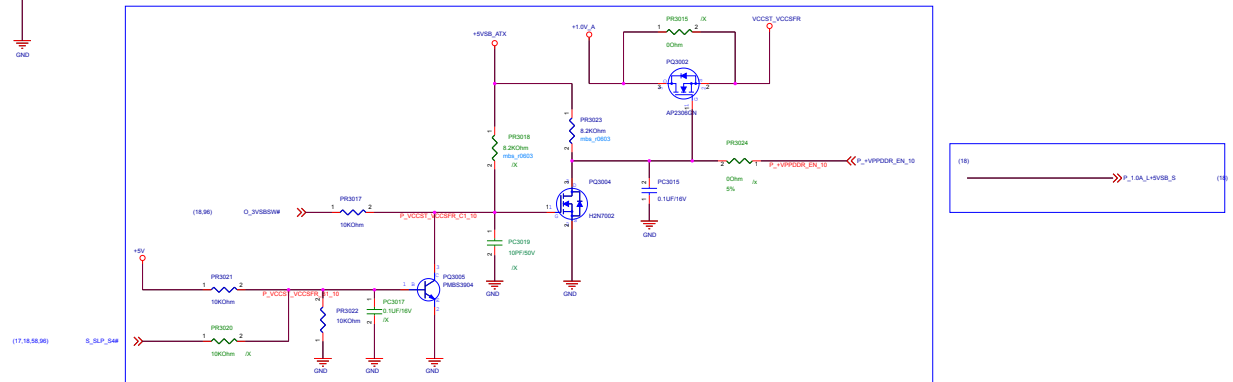


If IC is NB671LB, then PR300's optional is N/A.  
If IC is RT6220A, then PR300's optional is /X.



PR3013 ----50mV/step,1 step

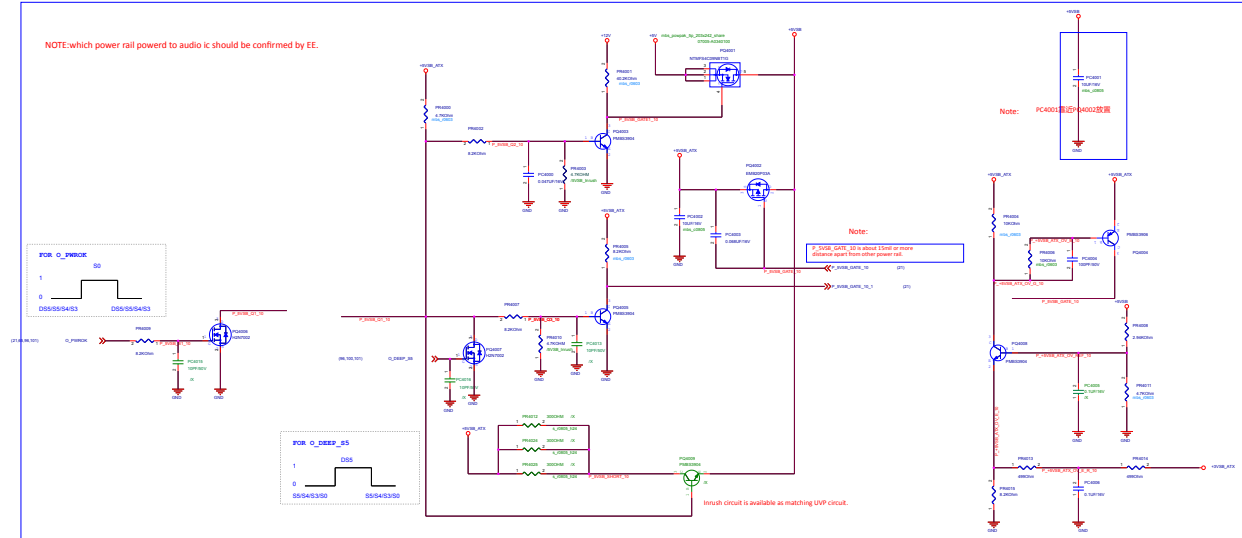
PR3013 —50mV/step,1 step		
P_+1.0V_A_OV#_1_10	+1.0V_A show value	+1.0V_A design value
1	1.00V	1.008V(default)
0	1.05V	1.0595V



(18)

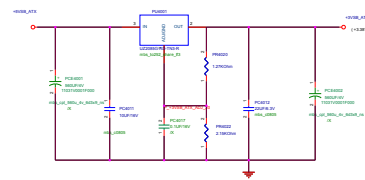
(74)

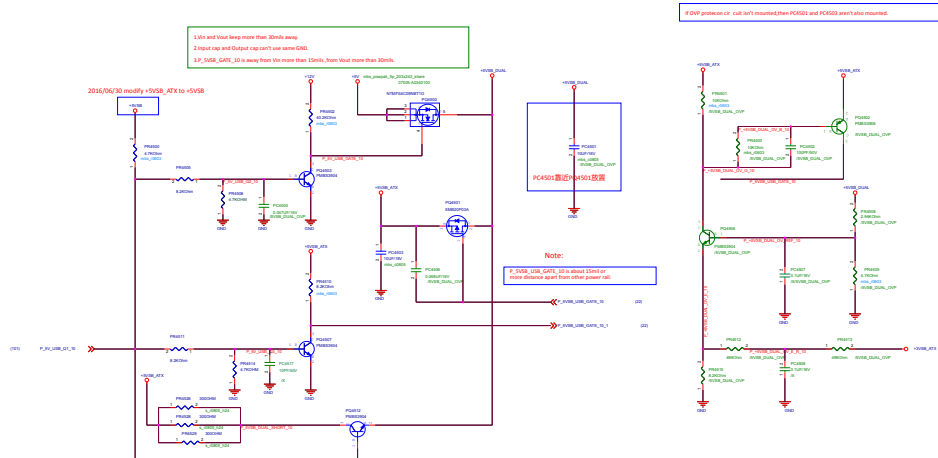
If OVP protecon cir. cult isn't mounted, then PC4001 and PC4002 aren't also mounted



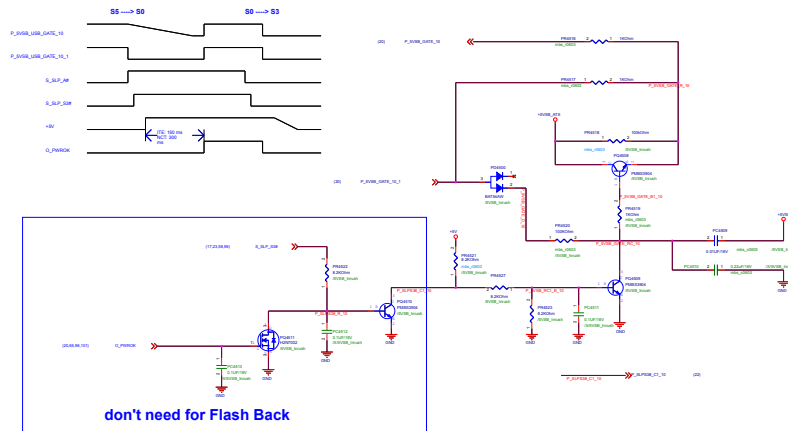
+5VSB ATX ==>+3VSB ATX

$I_o: 1.5A$



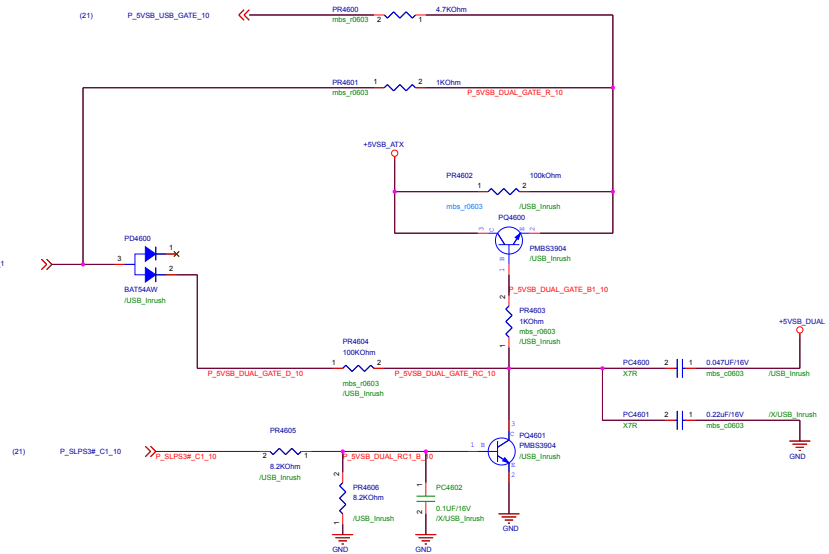
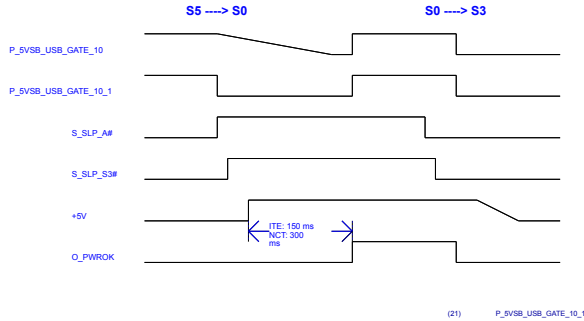


### Inrush Circuit for USB Port default have Power or Flash Back Function





### +5VSB\_DUAL Inrush Circuit for USB Port default have Power

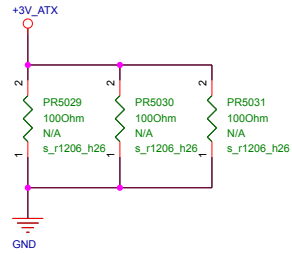
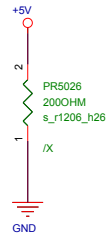




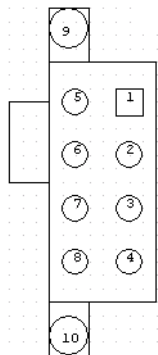
+3V\_ATX

+3V

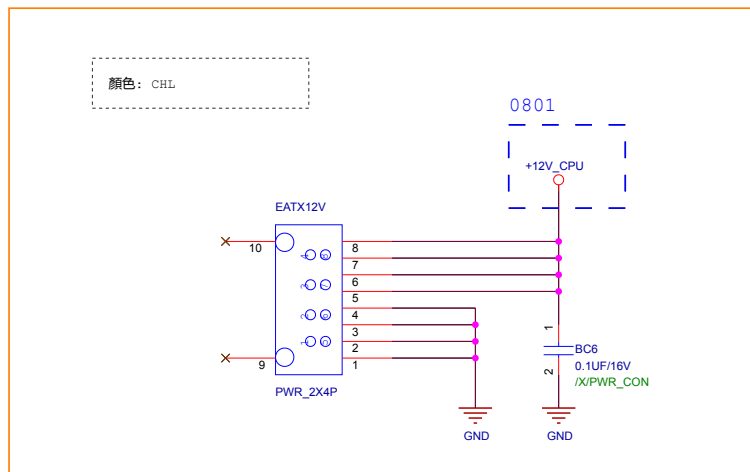


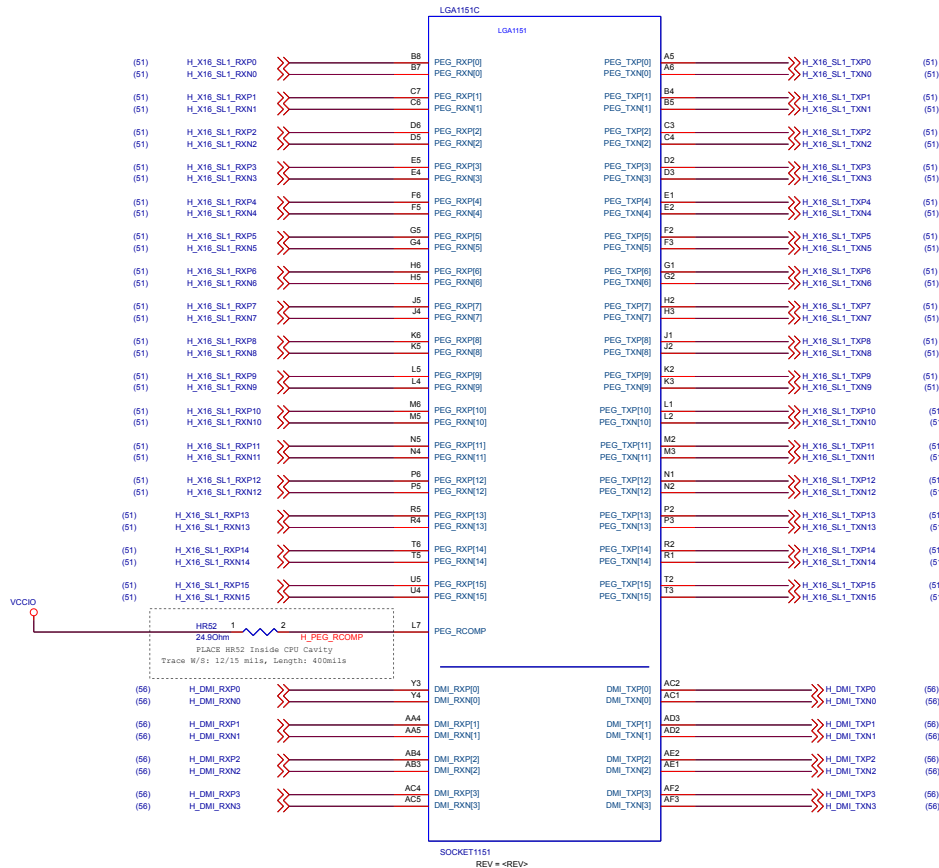


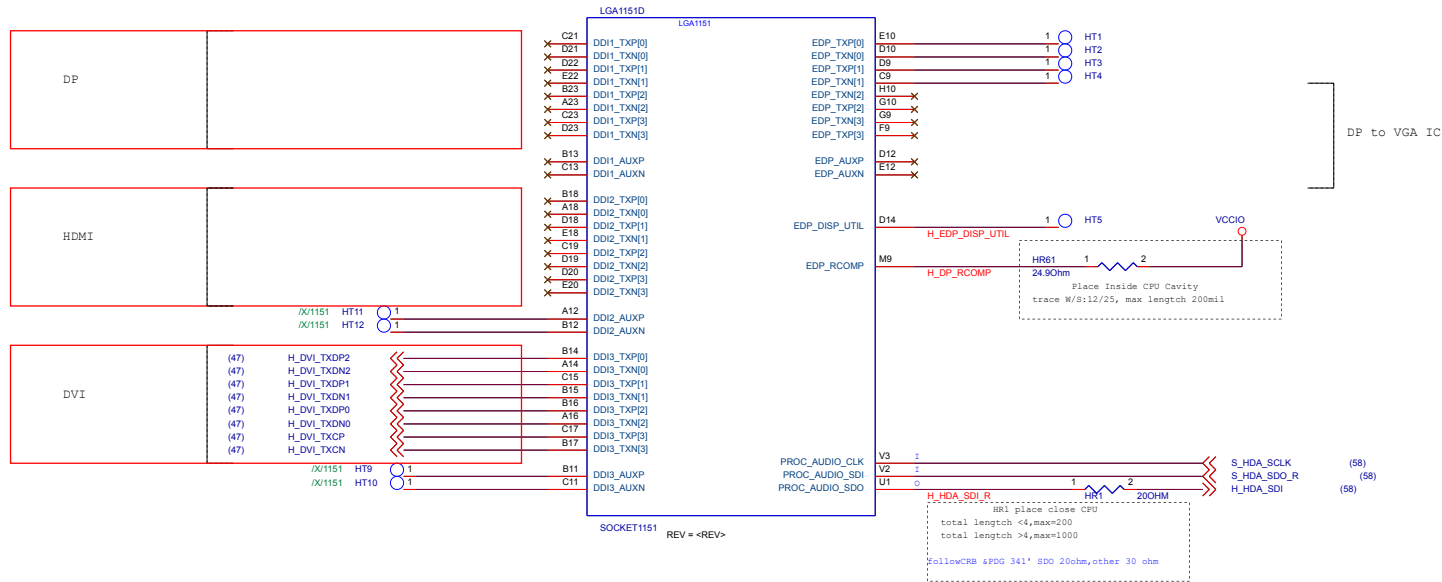
DUMMY LOAD



## 8 Pin +12V Connector

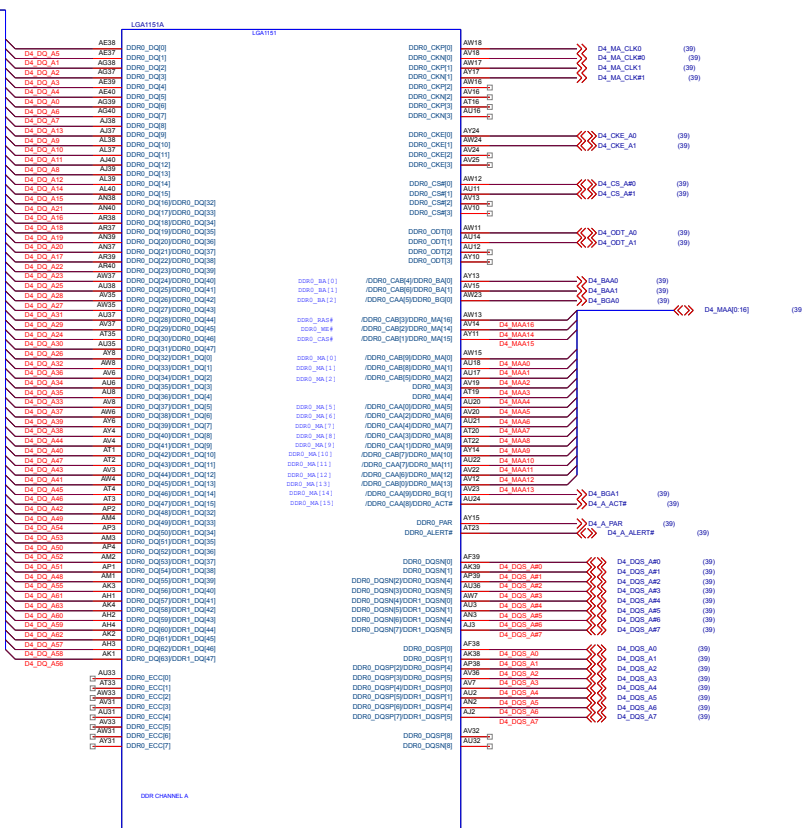






```
Channel A
4 Layer routing
```

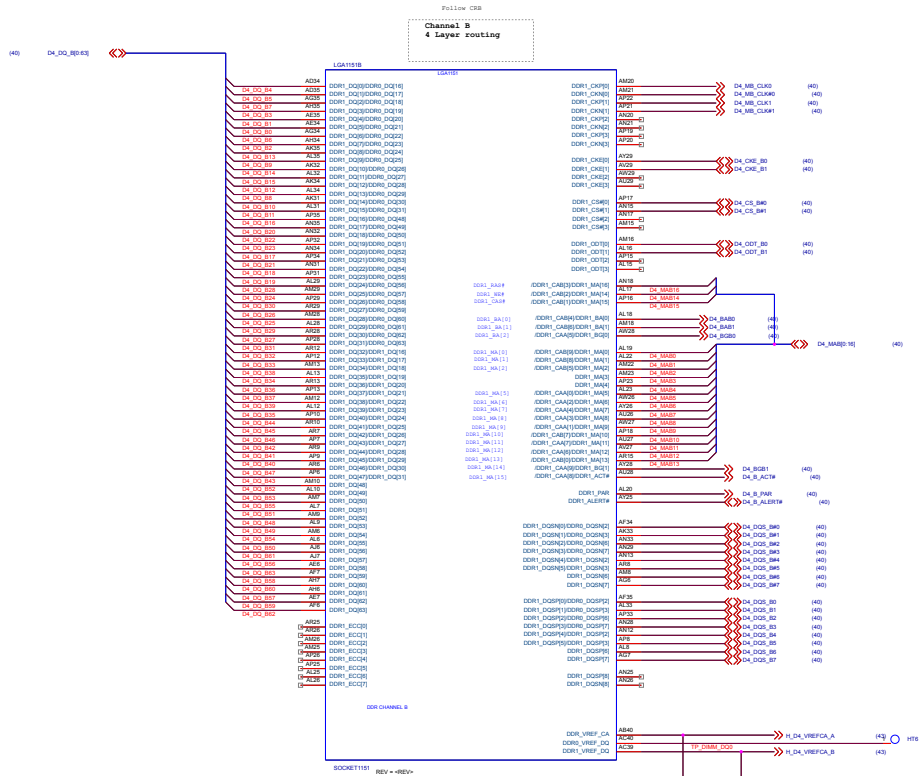
(39) D4\_DQ\_A[0:63] 



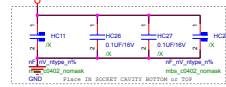
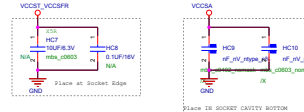
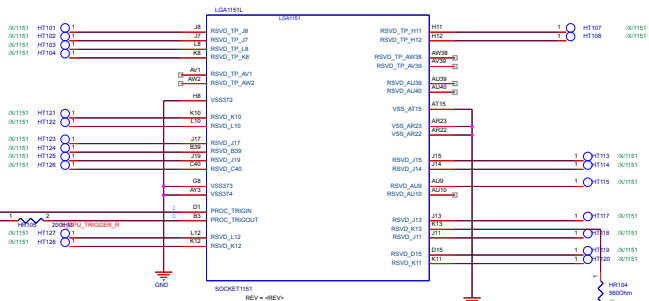
DOR CHANNEL A

SOCKET1151

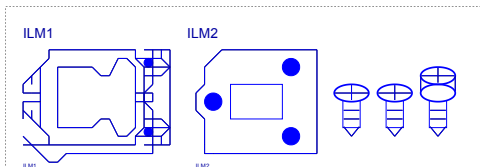




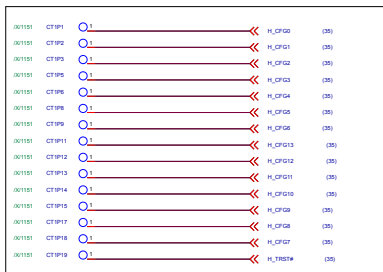




Place IN SOCKET CAVITY BOTTOM



XDP Card USB3 CON1



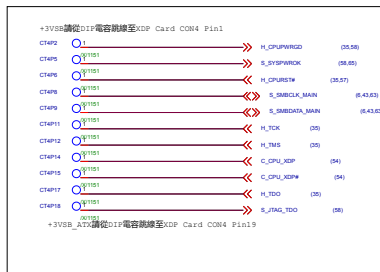
XDP Card USB3 CON2



XDP Card USB3 CON3



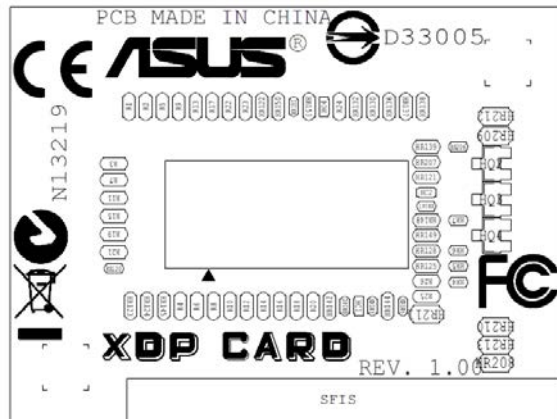
XDP Card USB3 CON4



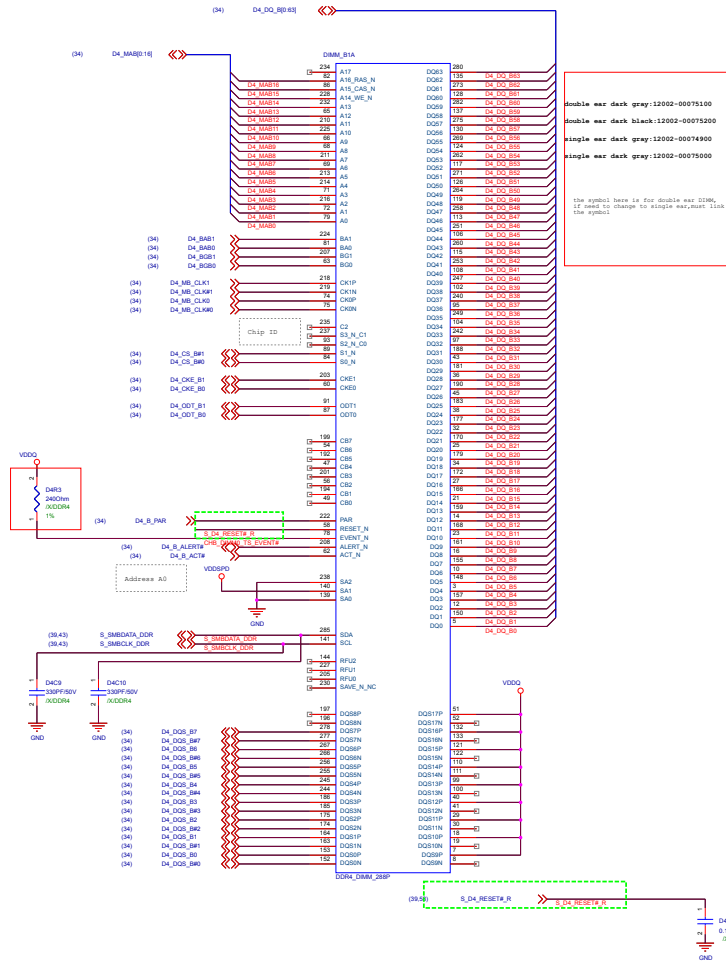
Naming Rule:  
C1xPy=>請將線到XDP Card CONx connector的PinY

Placement Rule:  
此頁面則貼全部放置位置最近輸出。  
Layout 會依照把Reference文字圖開出。  
若有需求初期PCB版本可洗背圖文字。  
但低階機種PVT PCB版本請記得通知板廠不洗背圖文字

Power Network:  
+1.0V\_A 請從D11電容網線至XDP Card CON2 Pin19  
+3VSB 請從D11電容網線至XDP Card CON4 Pin19  
+VCC10 請從D11電容網線至XDP Card CON3 Pin19  
+VCC10 請從D11電容網線至XDP Card CON2 Pin1  
+3VSB\_ATT 請從D11電容網線至XDP Card CON4 Pin19  
GND 請將線至XDP Card CON2 Pin7



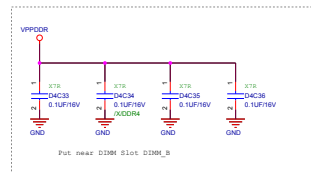
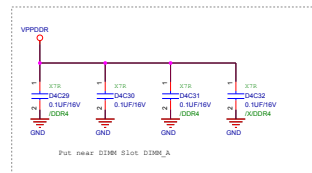
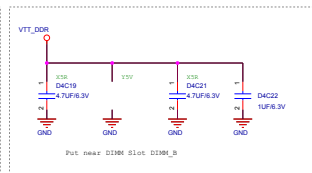
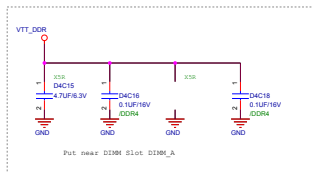
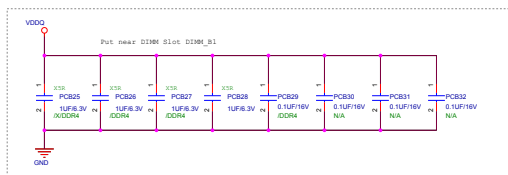
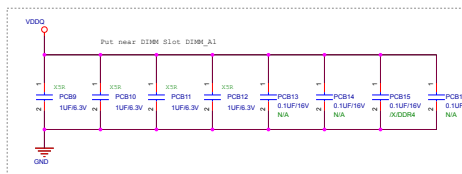
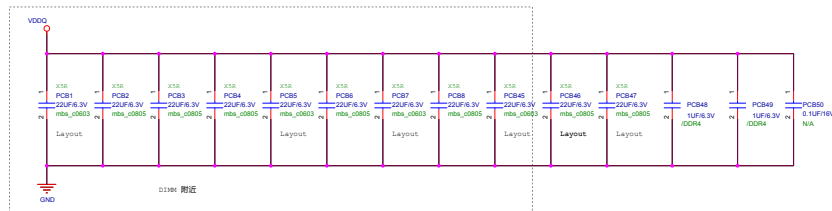








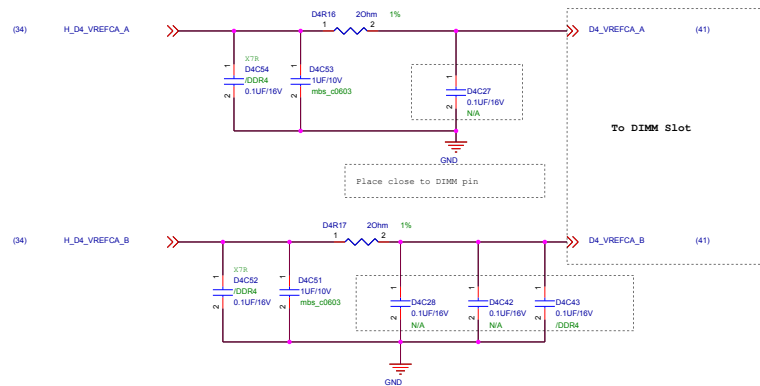
Layout to D603



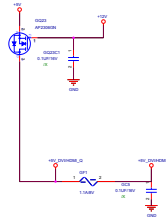


## CPU DDR Vref

For CPU DDR Vref

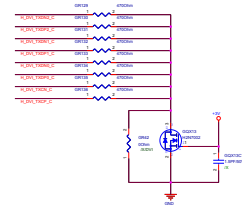
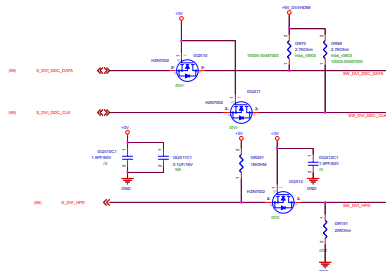


delete if  
sum > 0

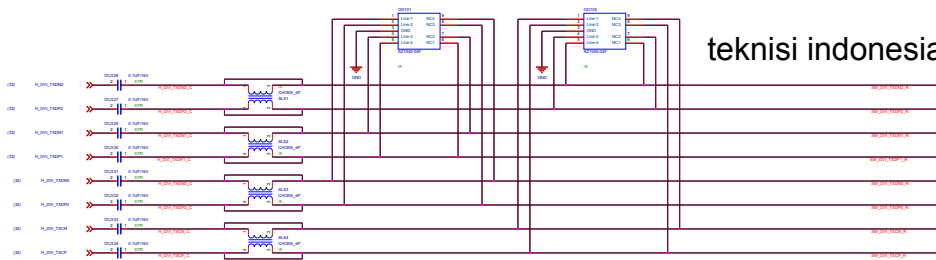


POWER for HDMI & DVI

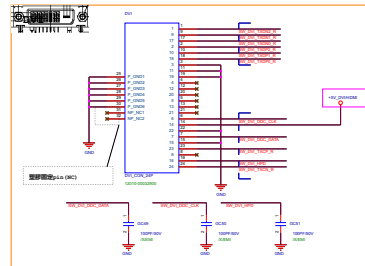
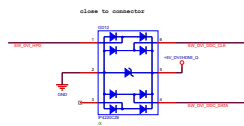
If only HDMI, this power must still need



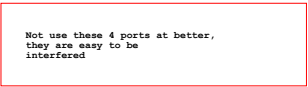
Passive/Active Devices					
Max Capacitance (Backdrive 1 Protection)	Schottky Diode	NA	pF	10	10
Resistor Value (+/- 5%)	R1/R2	NA	Ω	680	NA
ESD Protection	ESD	NA	NA	Optional	Optional
Max pFET Ron/Cold	NA	NA	120pF	3ohm 10pF	NA

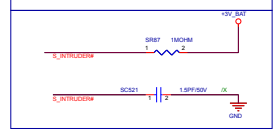
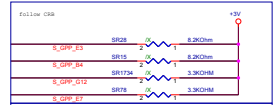
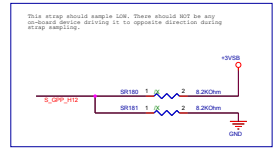
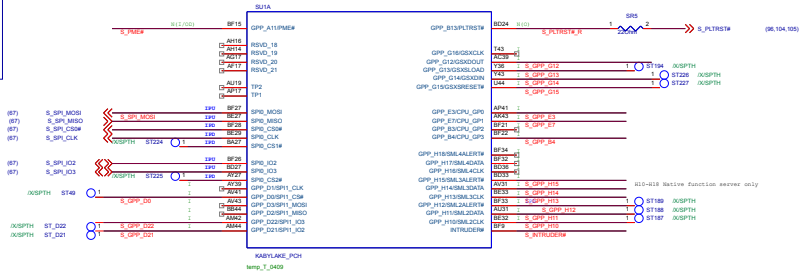
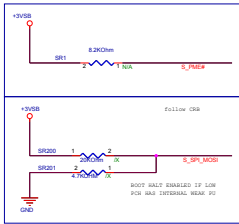


teknisi indonesia









for DUMMY load control

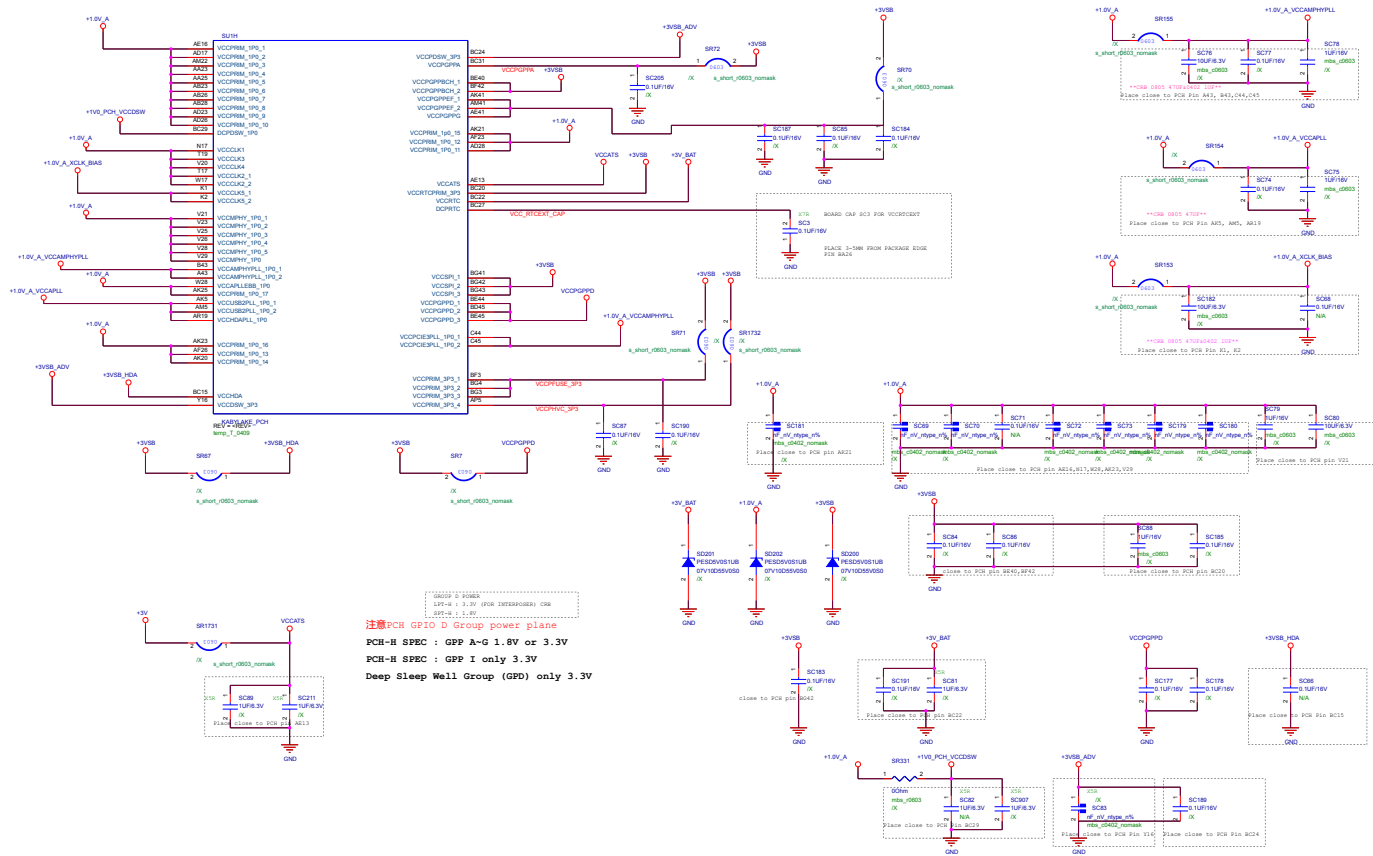




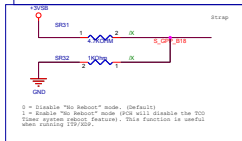








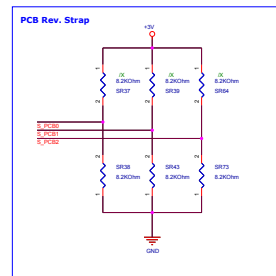


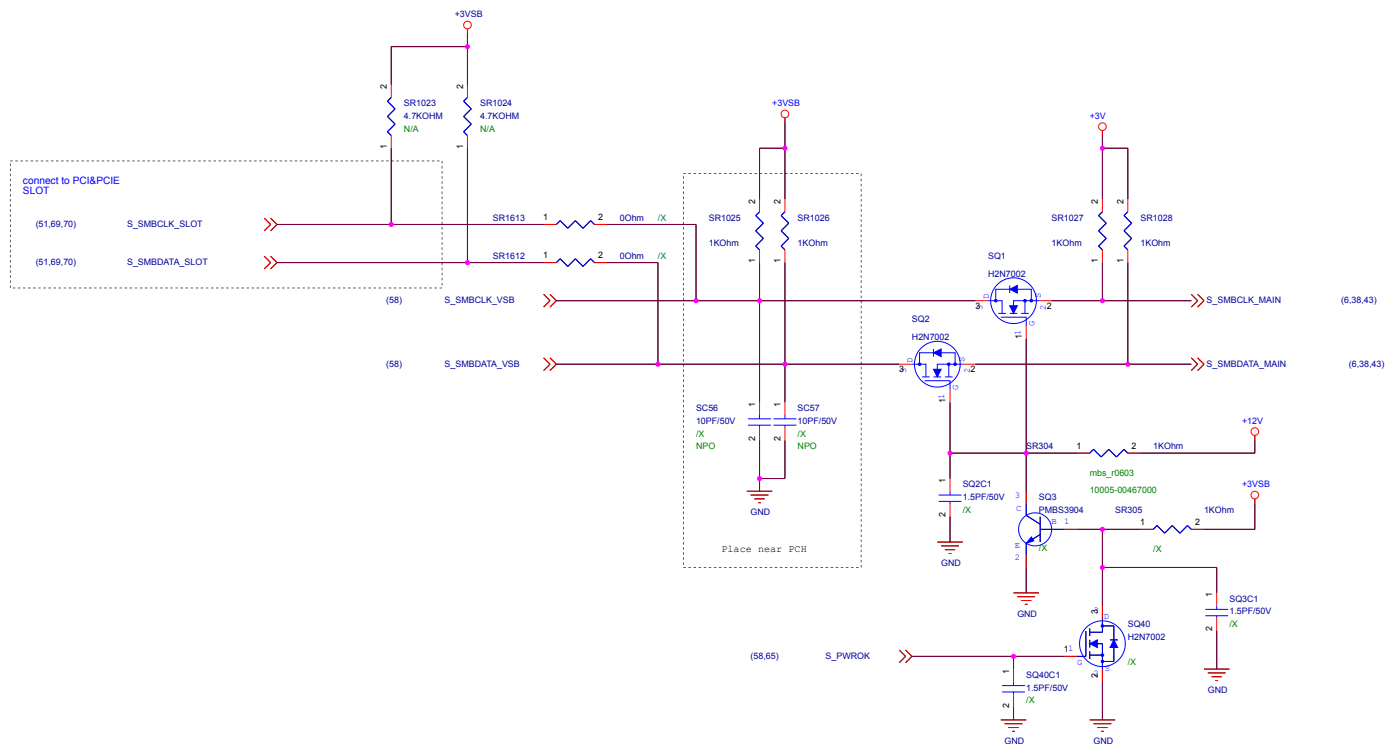


GPI PU

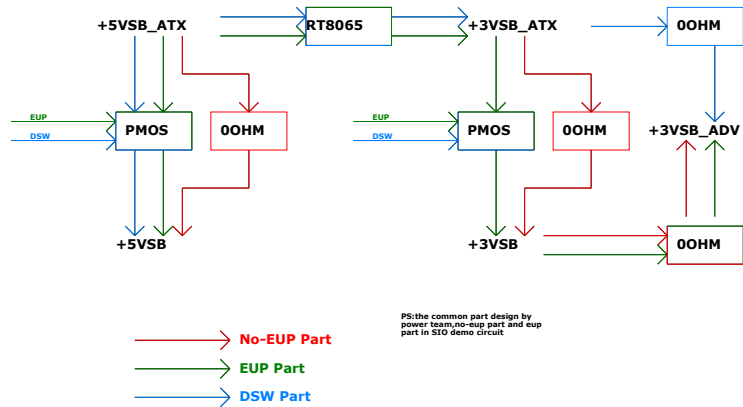
9:02 TYPSC PWR CTL 確認Demo pull up 基板仕様

\*\*\* C19 please change rate to project need



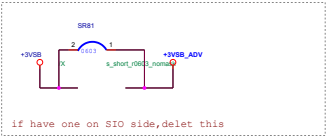


POWER FLOW



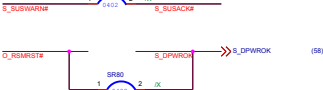
NOT SUPPORT DSW

Power plane



if NO DSW , please use shortpin

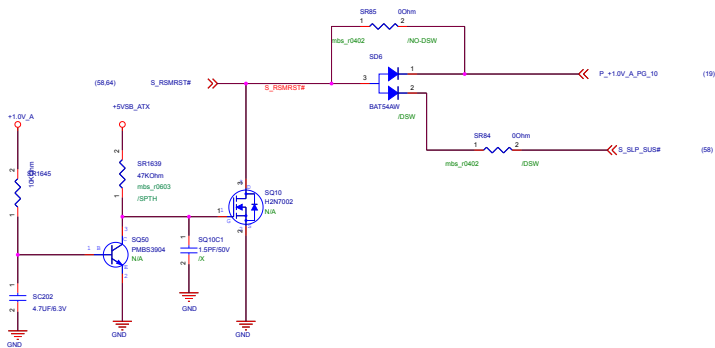
Control link



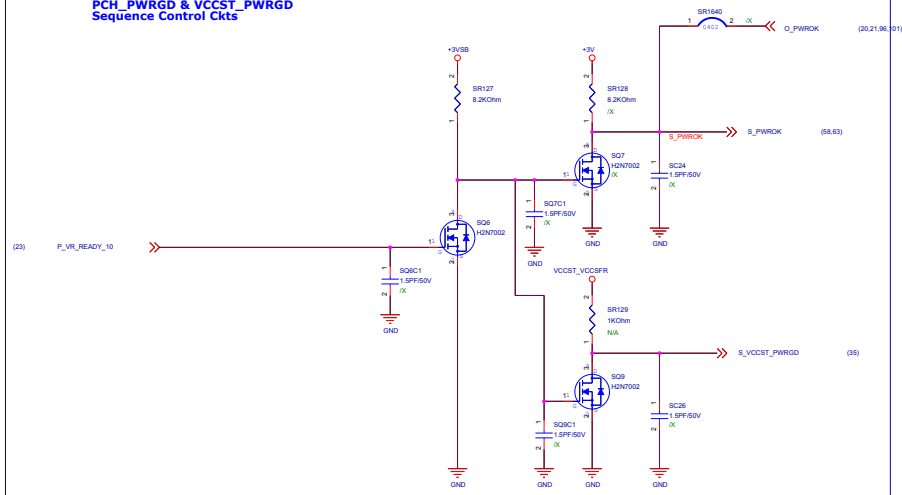
SUPPORT DSW

Power plane

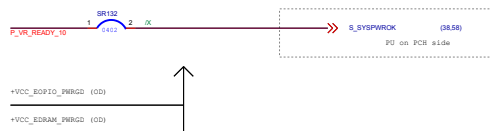
Control link



## PCH\_PWRGD & VCCST\_PWRGD Sequence Control Ckts



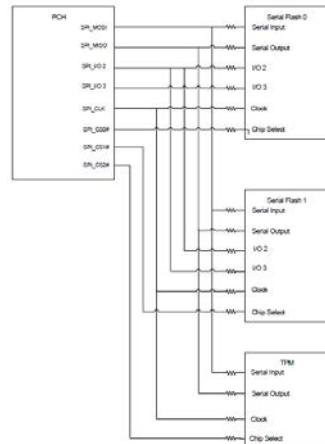
## PCH\_SYSPWROK Sequence Control Ckts

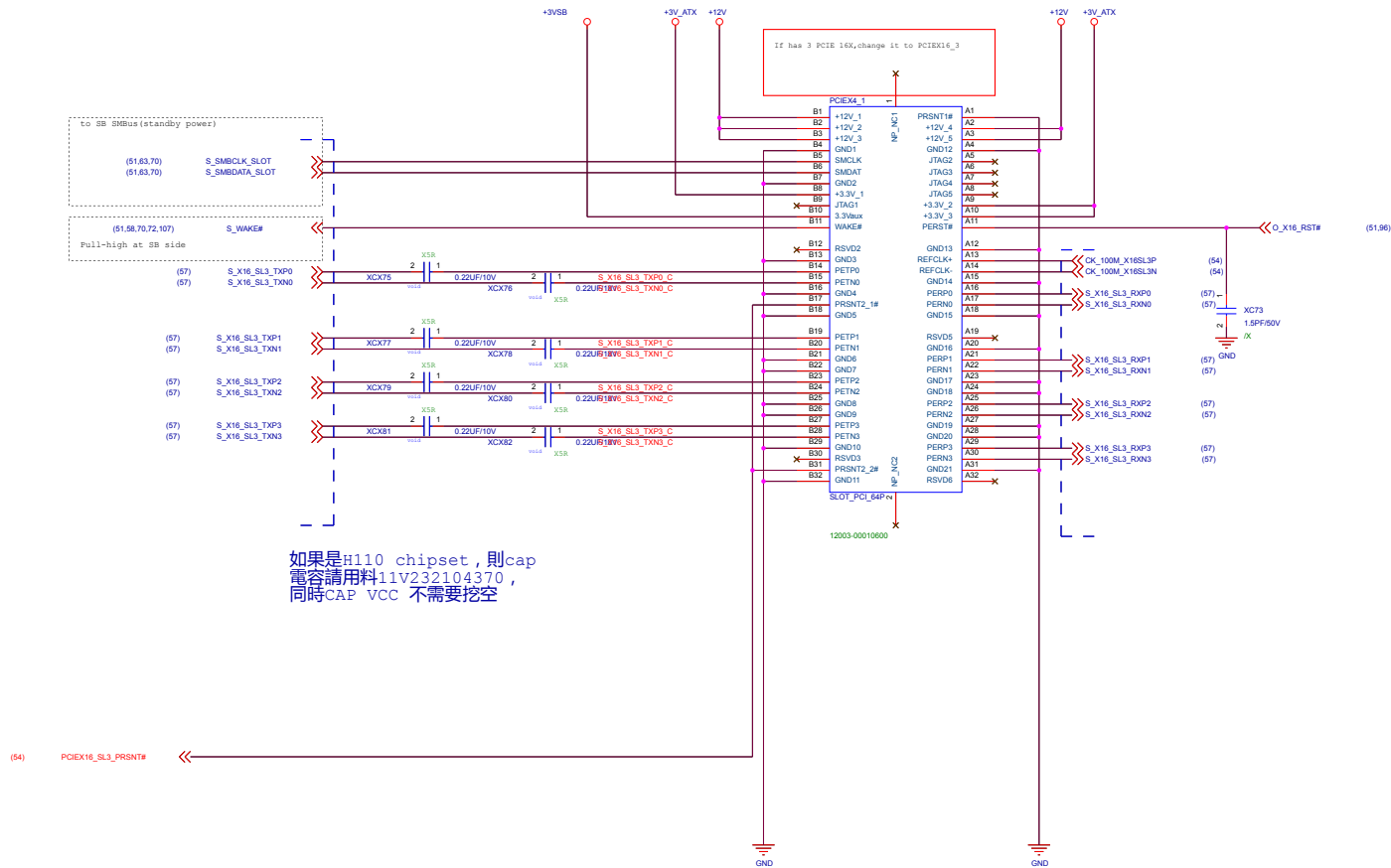


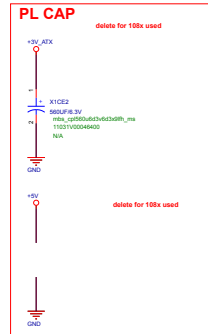
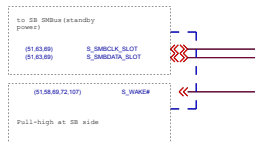
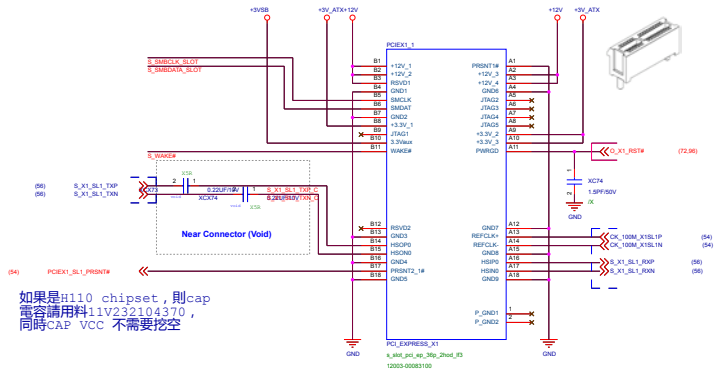
1. PCH will have a minimum of a 1ms delay from PCH PWROK to assertion of PROCWROGD.
2. P\_VR\_READY\_10 AND (PCH PWROK, SYS PWROK, PROCWROGD) Refer to PDC Figure 40-1 SBL S Flow Diagram for SYS PWROK/PCH PWROK Generation.
3. It is recommended that SYS PWROK be asserted after both PWROK assertion and processor PCH does not monitor.
4. PCH PWROK and SYS PWROK both needs to be high to exit reset, but either signal can come up first. SYS PWROK be asserted after both PWROK assertion and processor core VR PWROGD assertion.

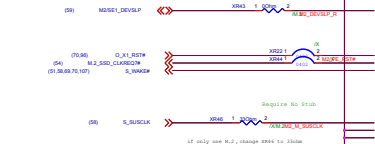
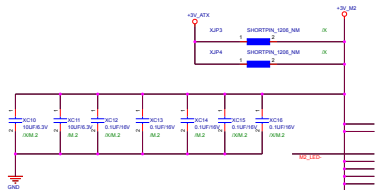


Standard Circuit	
BIOS	SPI
REV.	F1_0.3G_Data









Regulator No Switch

If only use M.2, change M2\_4 to 100K

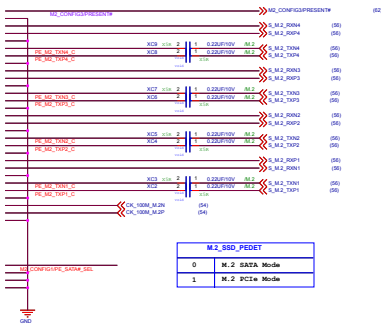
If only use M.2, change M.2 to M.2 (SECRET3)

M.2 SECRET3

M.2\_100

12001-0071000

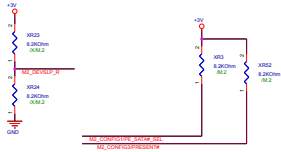
M.2

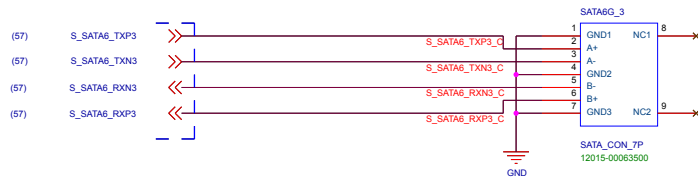


M.2 SSD_FDET	
0	M.2 SATA Mode
1	M.2 PCIe Mode

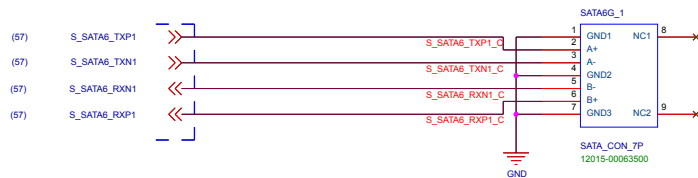


BOM P/N: 13020-01370000





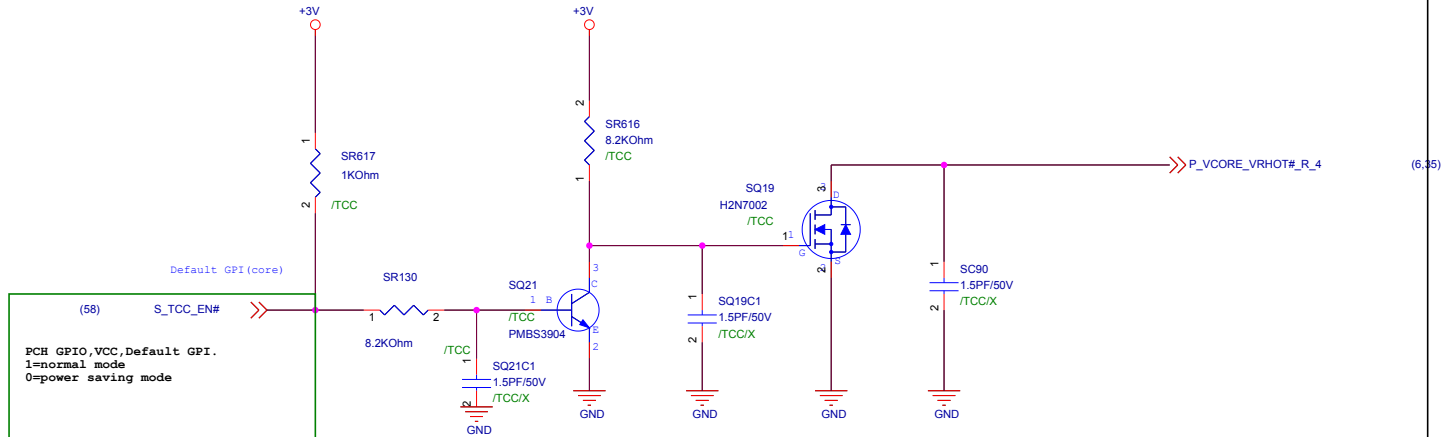
## 180度connector



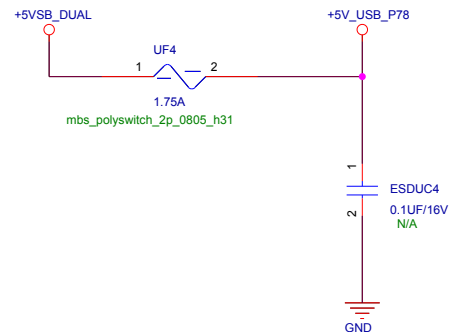
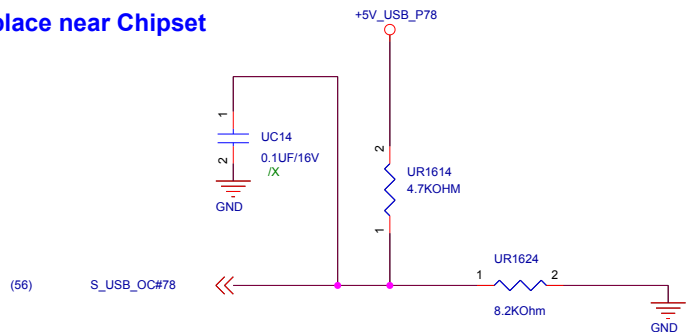
## 180度connector



## TCC control

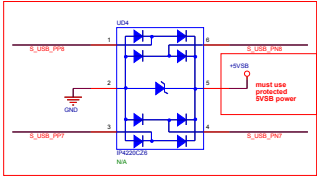


place near Chipset



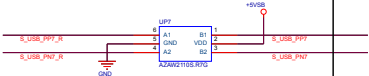
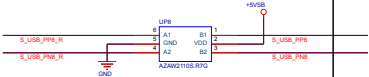
Delete it for EMS

ESD Diode



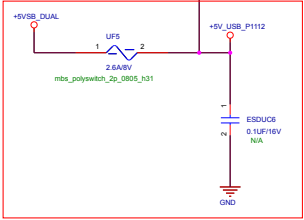
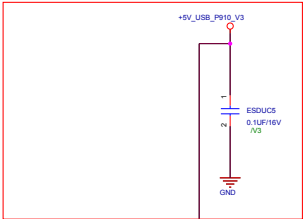
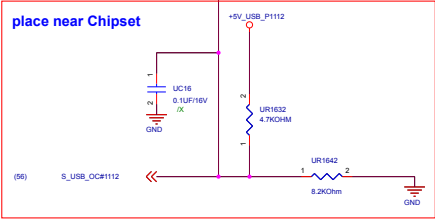
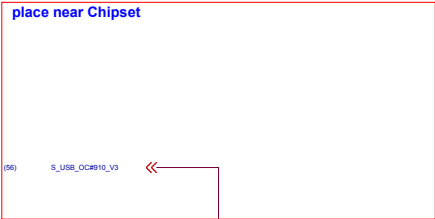
Delete it for EMS

2nd ESD Diode for Skylake

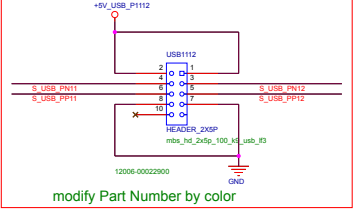
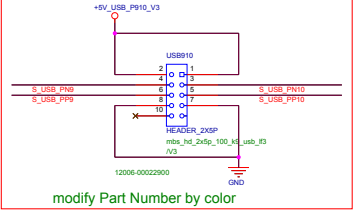




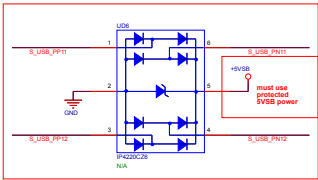
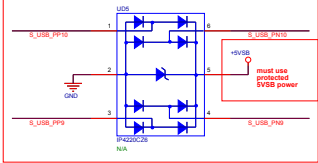
OC# circuit for Intel



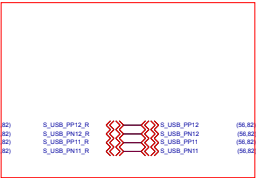
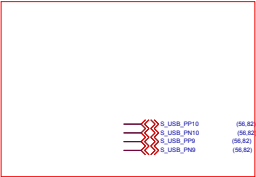
USB2 Header



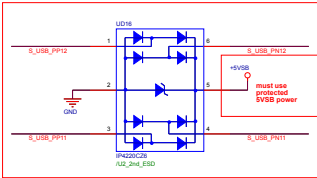
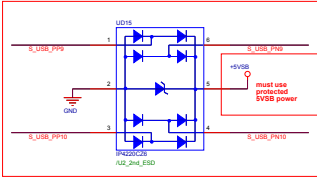
# ESD Diode



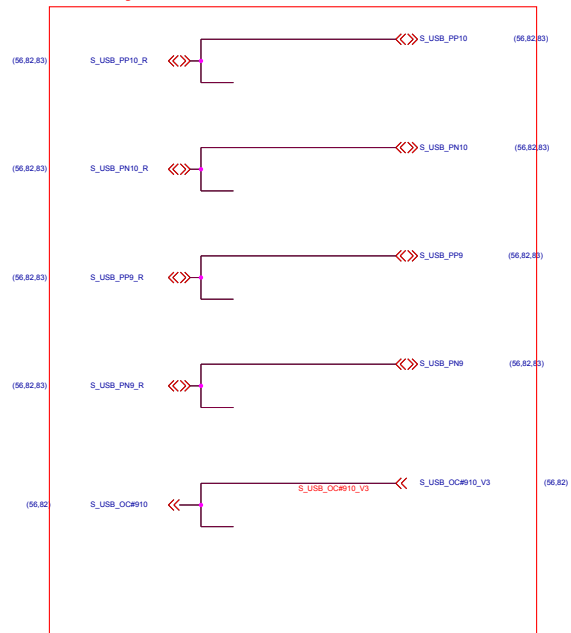
# No EMI Choke



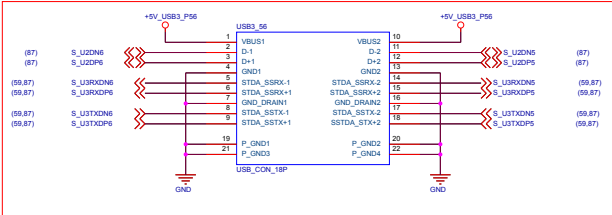
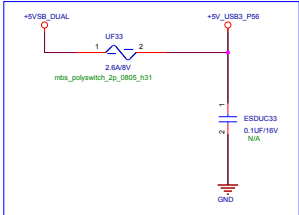
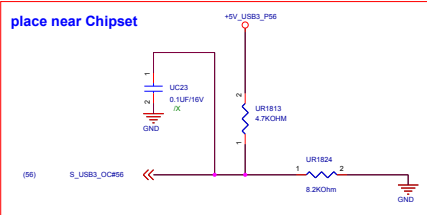
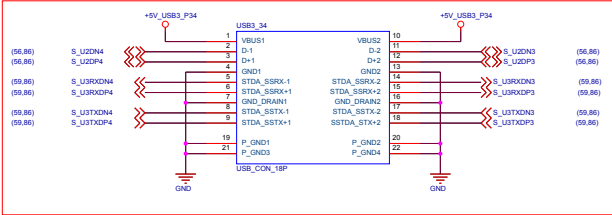
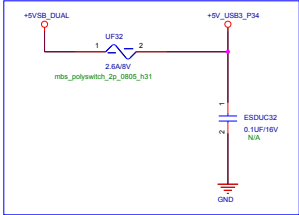
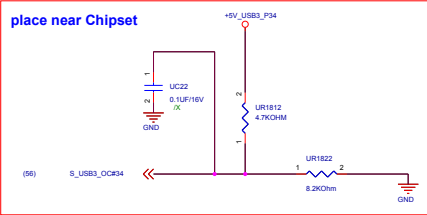
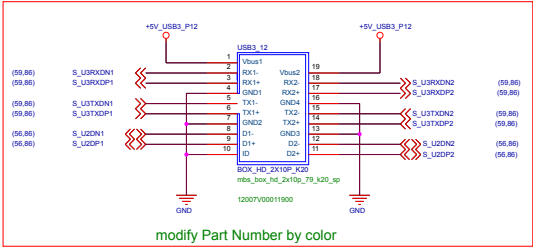
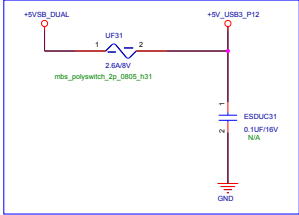
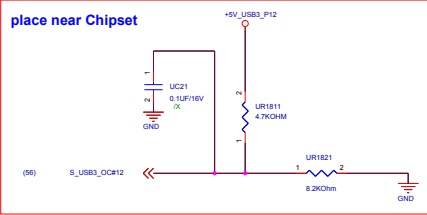
# 2nd ESD Diode for Skylake



## Co-lay



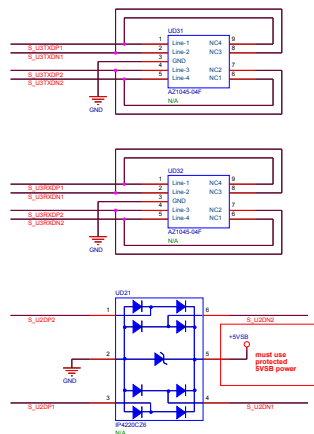
OC# circuit for Intel



# Port 12

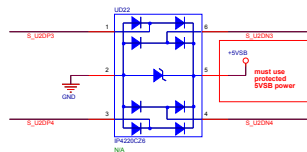
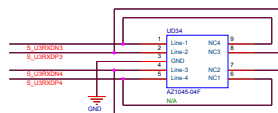
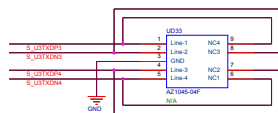
Delete it for EIS

## ESD Diode

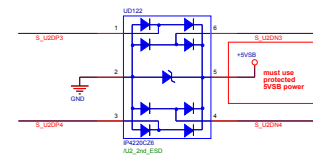
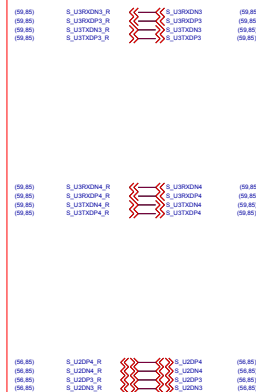


Delete it for EIS

## ESD Diode



## No EMI Choke

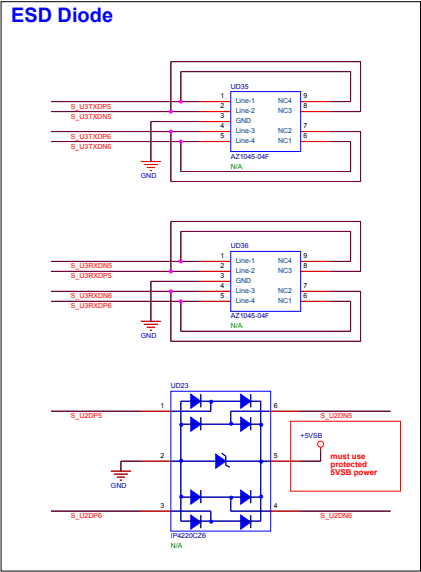


# Port 34

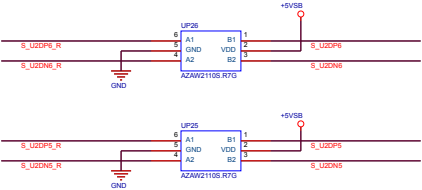
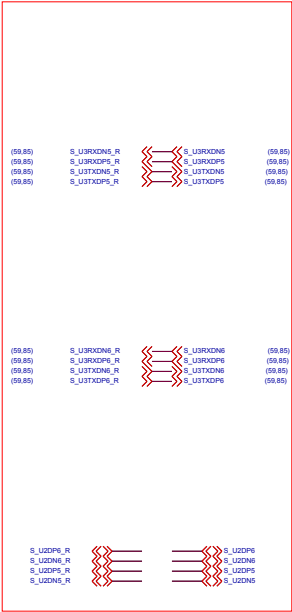
# Port 56

Delete it for EMS

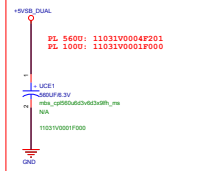
## ESD Diode



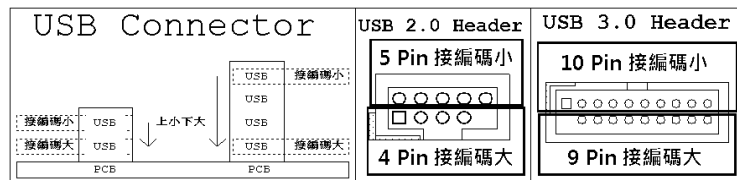
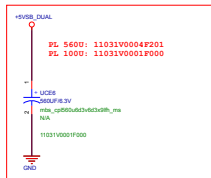
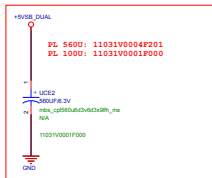
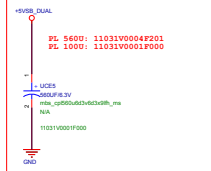
## No EMI Choke



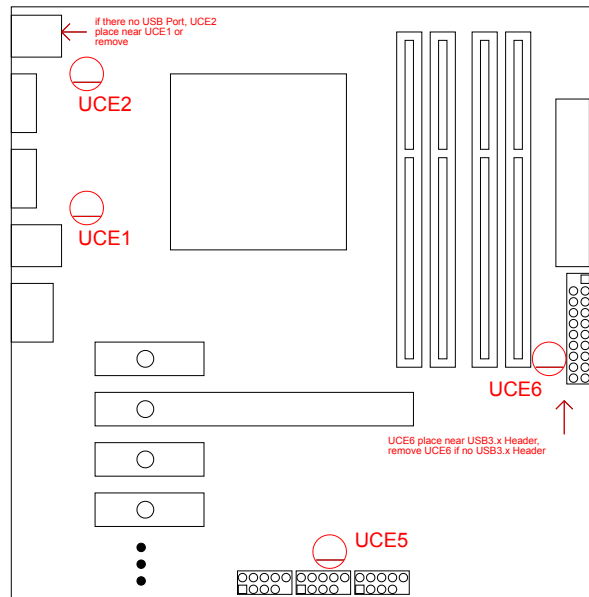
# PL CAP



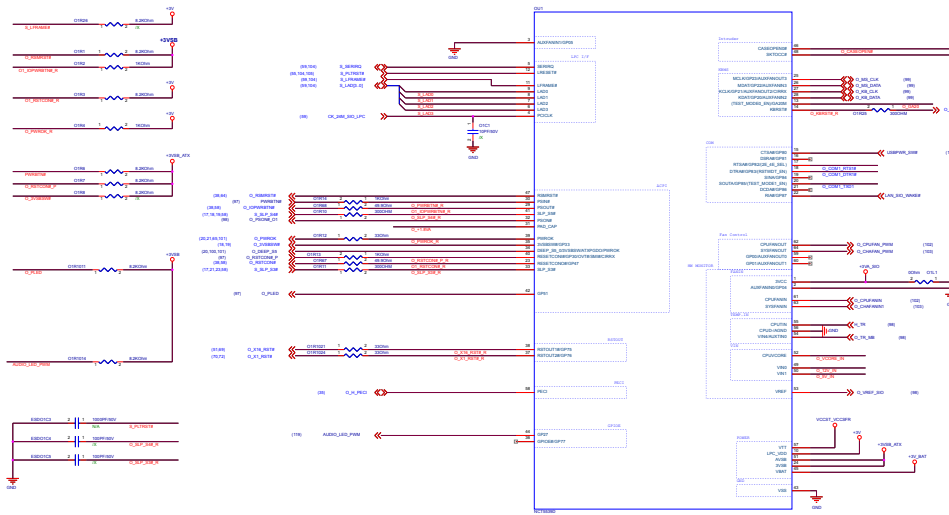
# PL CAP



## USB Power CAP recommend placement

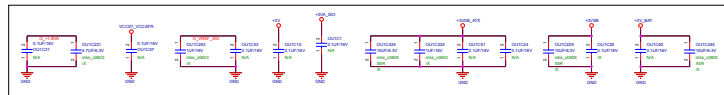
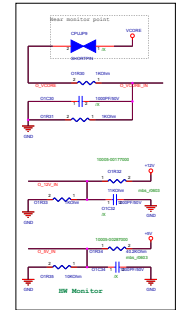


# LPC Bus: check Chipset internal pull-high

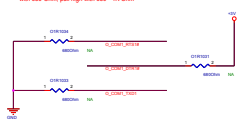


FAN	Sense	Speed Control
FAN1	CL_FANSENSE1	CL_FANCTRL1
FAN2	CL_FANSENSE2	CL_FANCTRL2
FAN3	CL_FANSENSE3	CL_FANCTRL3
FAN4	CL_FANSENSE4	CL_FANCTRL4
FAN5	CL_FANSENSE5	CL_FANCTRL5
FAN6	CL_FANSENSE6	CL_FANCTRL6

1. unused TRN connected to GND
2. unused TRN (no TRN multi-function) be to GND
3. unused FANIN be to GND



Nonzero BOD COM Pin Strapping Pin pull down with 680 Ohm pull high with 680k Ohm



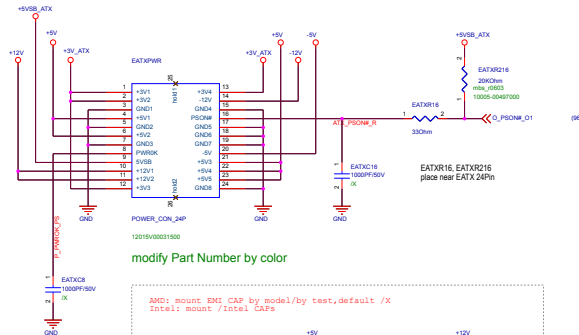
ROW	COL
1A	1B
1C	1D

STANDARD CIRCUIT
1A
1B
1C
1D



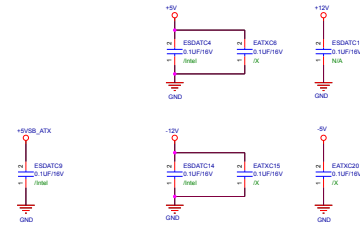


## EATX POWER



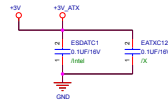
modify Part Number by color

AMD: mount EM2 CAP by model/by test,default /X  
Intel: mount /Intel CAPs

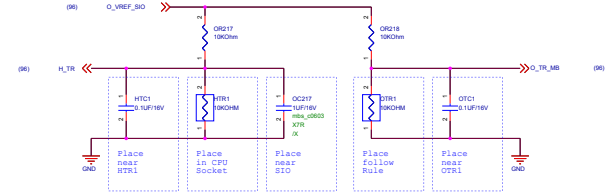


place near EATXPWR

for no +3V OVP  
Protect Circuit



## HW Monitor



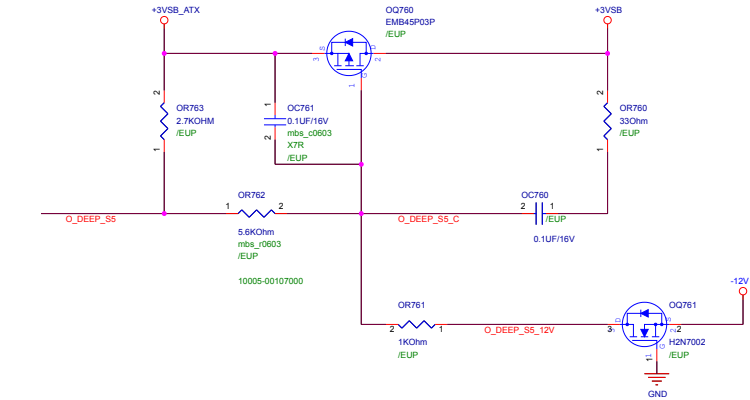
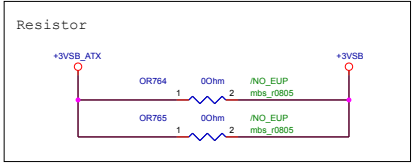
If no CPU thermistor, unmount components HTR1, OC430, OR431

If no MB thermistor, unmount components OTR1, OC432, OR433

[illegible]

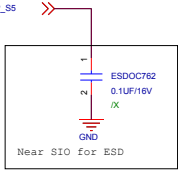
BOM	no SIO ERP & SIO DSW	SIO ERP	SIO DSW
/NO_EUP	mount	unmount	unmount
/EUP	unmount	mount	mount
/NO_SIODSW	mount	mount	unmount
/SIODSW	unmount	unmount	mount

# ERP Circuit



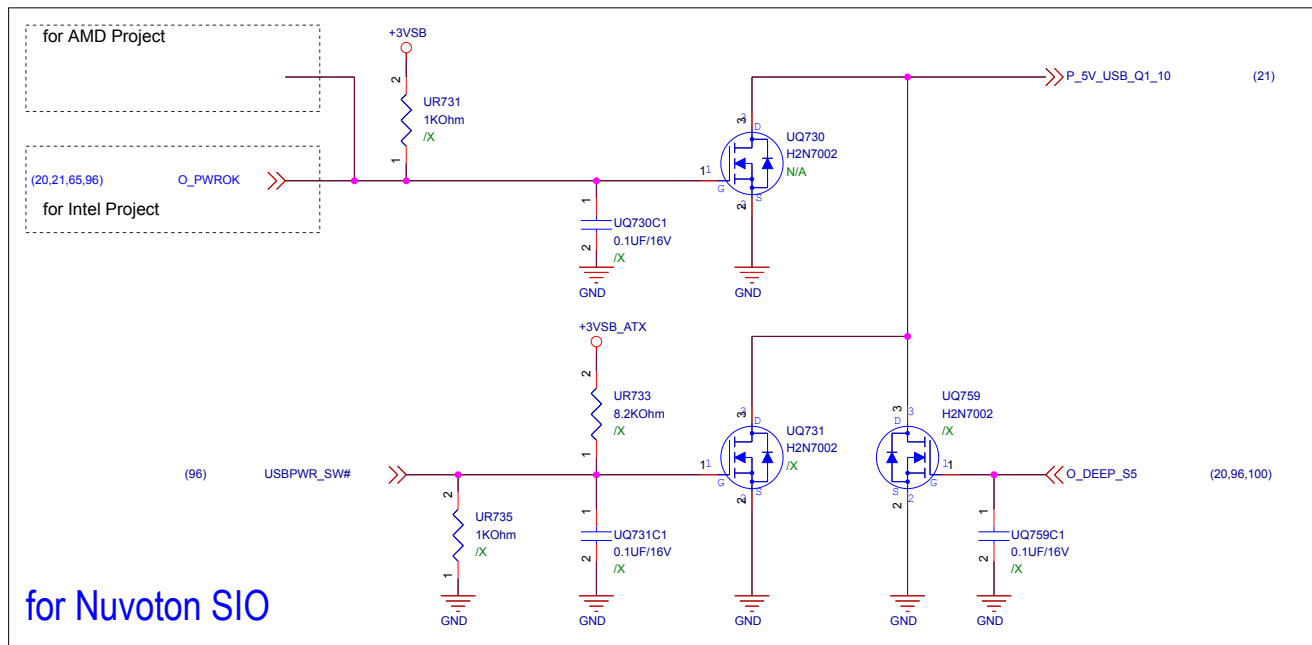
(20,96,101)

O\_DEEP\_SS



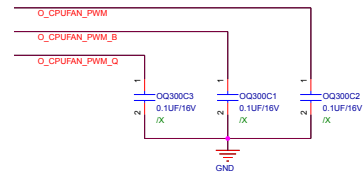
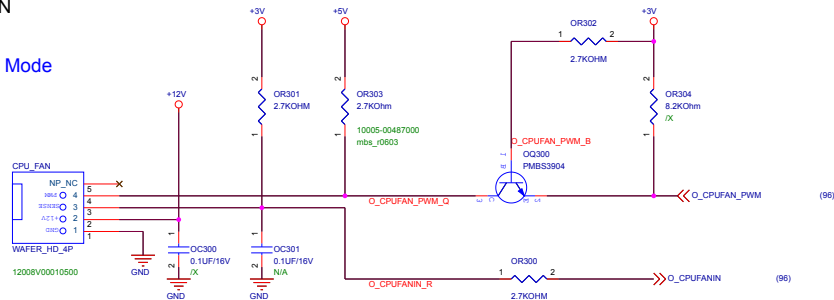
# No ERP Circuit

+5VSB\_DUAL default power on, don't need GPIO control

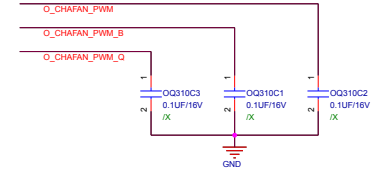
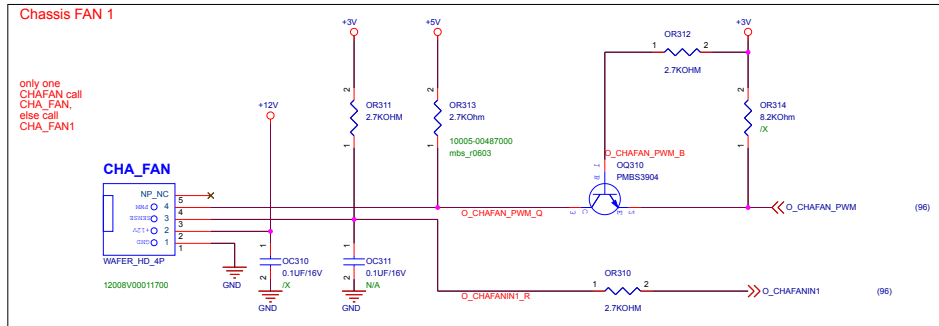


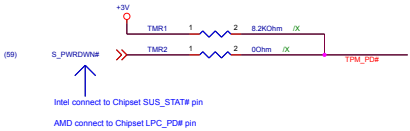
## CPU FAN

### PWM Mode

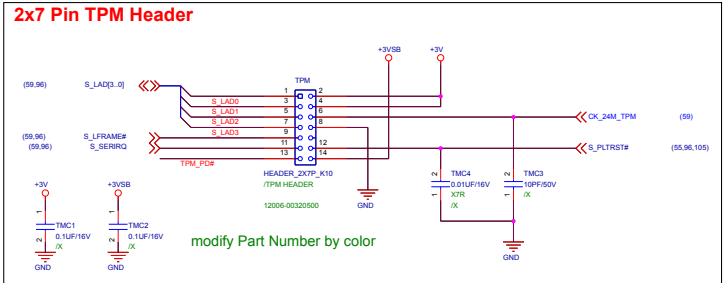


## 4 Pin PWM Mode



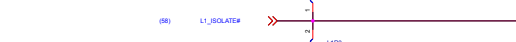


Delete it for EMS

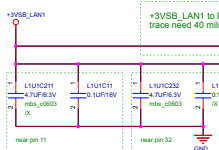


BOM	TPM Header	Onboard TPM
N/A	mount	mount
/X	unmount	unmount
/TPM HEADER	mount	unmount
/TPM IC	unmount	mount





- L1\_ISOLATE GPIO select:**
- could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
  - main power plane or stand by power plane, 3V tolerance
  - GPI to enable Realtek LAN
  - GPO low to disable Realtek LAN



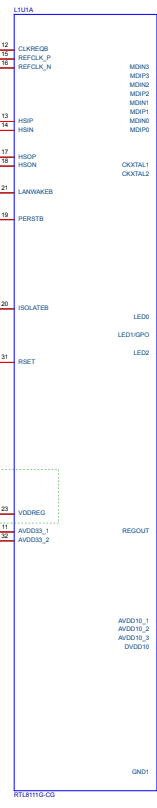
STANDARD CIRCUIT	
CLKREQ_LAN1	LAN1
LAN1_RNP	LAN1
LAN1_TNP	LAN1
LAN1_TAN	LAN1
LAN1_RAN	LAN1
LAN1_WAKER	LAN1

BOM	
N/A	mount
/X	unmount

RTL8111G : 02043-00090900  
RTL8111GR : 02043-00090900  
RTL8111M : 02043-00091100

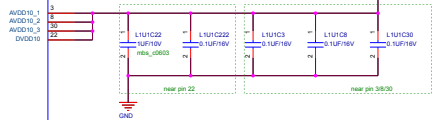
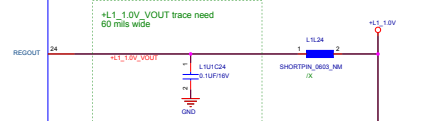
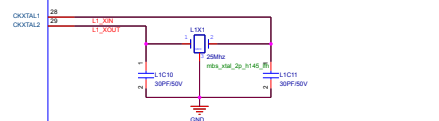
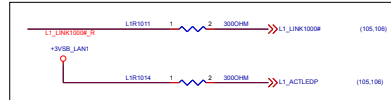


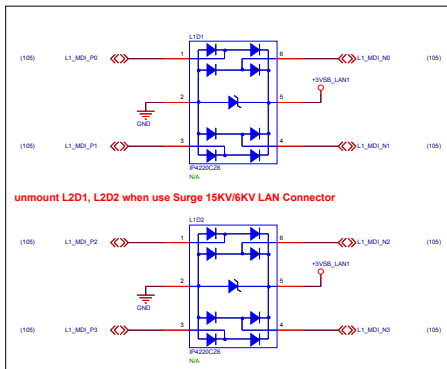
02043-00091100



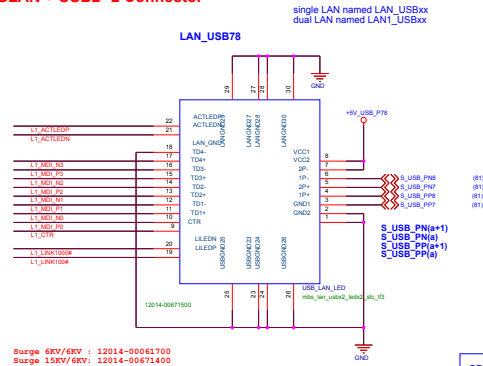
02043-00091100

# RES A





**GLAN + USB2 \*2 Connector**



**Intel LAN I217 should use old LAN Surge Connector**  
**U2+LAN Connector: 12014-00061500**  
**U3+LAN Connector: 12014-00061400**

## LAN1 POWER

1. LAN IC power change to +3VSB\_ATX (remove short-pin L1R88, add resistor L1R88 & L1R89)

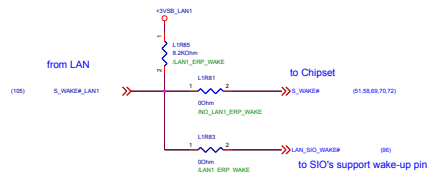


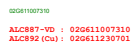
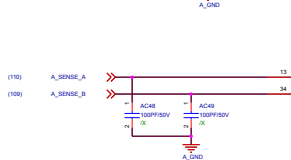
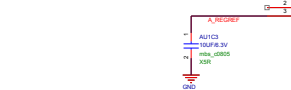
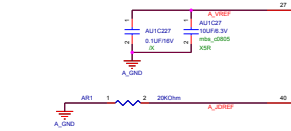
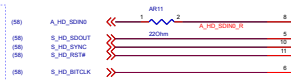
## for Intel PHY

2. for Intel PHY LAN, L1\_LAN\_DISABLE# renamed L1\_LAN\_DISABLE\_R in LAN IC Page
3. for Intel PHY LAN, L1\_LAN\_DISABLE# pull high resistor L1R7 Optional change to /LAN1\_ERP\_WAKE
4. for Intel PHY LAN, L1\_LAN\_WAKE# renamed L1\_LAN\_WAKE\_R in LAN IC Page

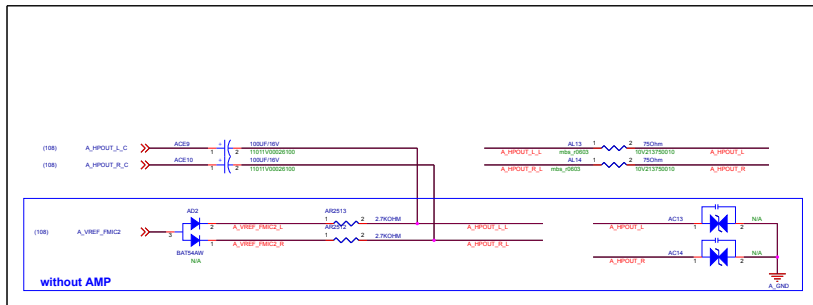
## for PCIE LAN1

5. for Intel PCIE LAN, L1\_DEV\_OFF# choose +3VSB\_ATX power plane GPIO
6. for PCIE LAN, S\_WAKE# renamed S\_WAKE#\_LAN1 in LAN IC Page





for  
ALC1200  
for ALC887-VD2/ALC892/ALC1150



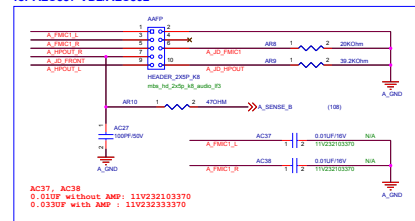
DIP CAP  
EL 1000 : 110040810743  
PL 1000 : 11031V0001P000  
Audio 1000 : 11011-00024000  
Gamez 1000 : 11011-00028000

AL13, AL14  
75 Ohm: 10V213750010  
47 Ohm: 10V213470010

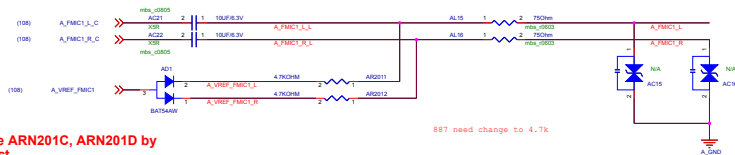
Audio 1000 Smm:11011V00026100

## AAFP

for ALC887-VD2/ALC892



AC37, AC38  
0.010F without AMP: 11V232103370  
0.0330F with AMP : 11V23233370



or use ARN201C, ARN201D by  
Project

887 need change to 4.7k

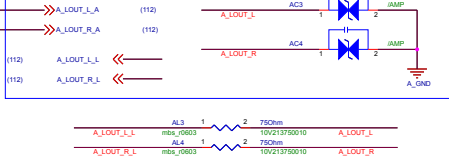
Delete it for EMS

Delete it for EMS

100UF

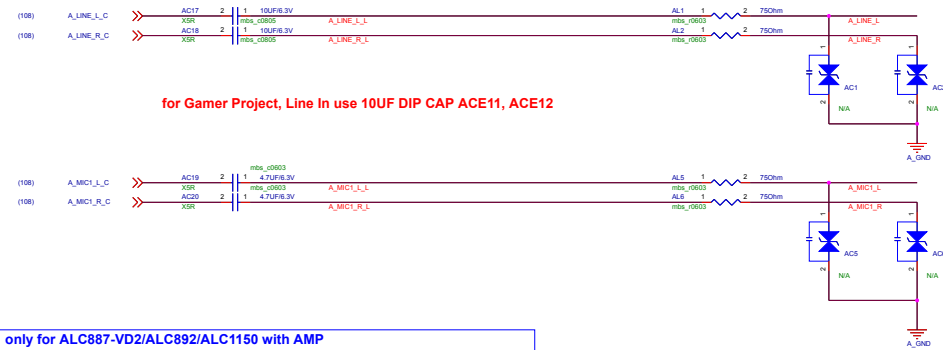


with AMP/De-POP

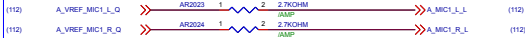


tekni indonesia

for Gamer Project, Line In use 10UF DIP CAP ACE11, ACE12

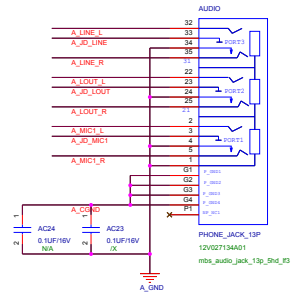


only for ALC887-VD2/ALC892/ALC1150 with AMP



DIP CAP  
EL 100 : 11G040822620  
PL 100 : 11V090106207  
Audio 100 : 11011-00066000  
Gamer 100 : 11011-00062000  
EL 1000 : 110040810743  
PL 1000 : 11031V00031P000  
Audio 1000 : 11011-00026000  
Gamer 1000 : 11011-00066000

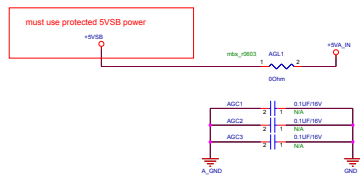
for ALC887-VD2/ALC892

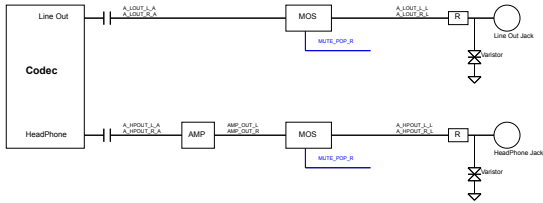


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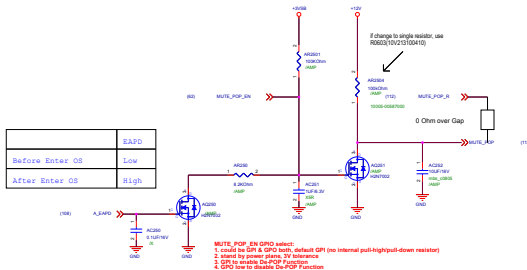
## 40 mils Gap for XU

0402 & 0603 component over 40 mils Gap must mount

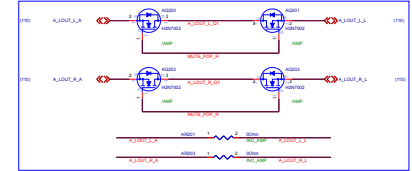




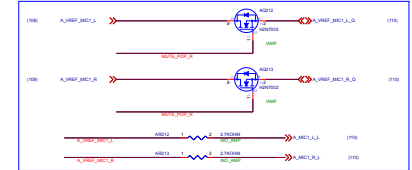
for ALC887-VD2/ALC892/ALC1150



for ACE1 & ACE2 use 100UF



only for ALC887-VD2/ALC892/ALC1150 Rear 3 Jacks



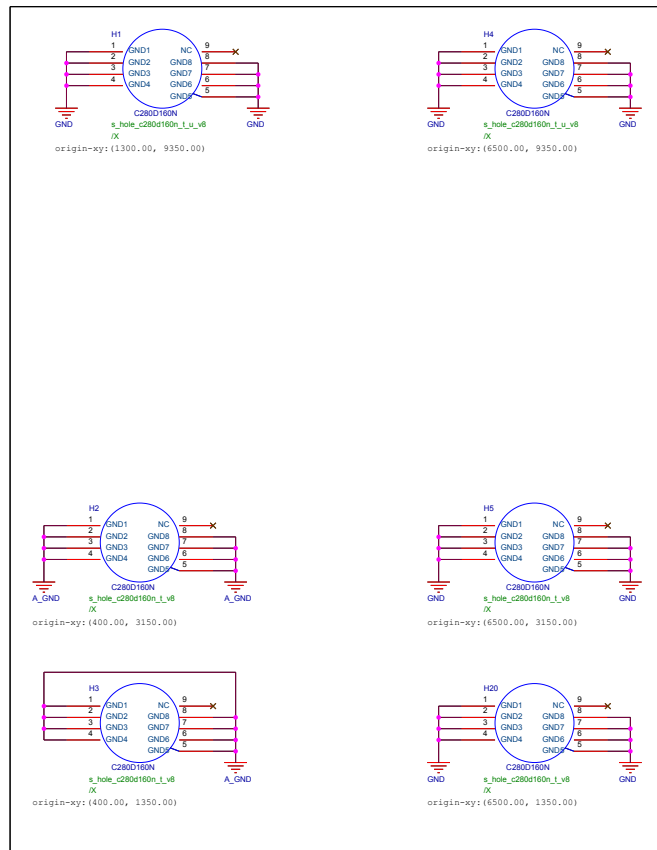


Delete it for EMS

# m-ATX Screw Hole

< 9.3 inch

(X,Y)=(0,0)



< 9.6 inch

## MB SCREW FOOTPRINT

MB\_HOLE\_160\_T\_LF3



MB\_HOLE\_160\_T\_U\_LF3



MB\_HOLE\_160\_T\_R\_LF3



MB\_HOLE\_160\_T\_UR\_LF3



